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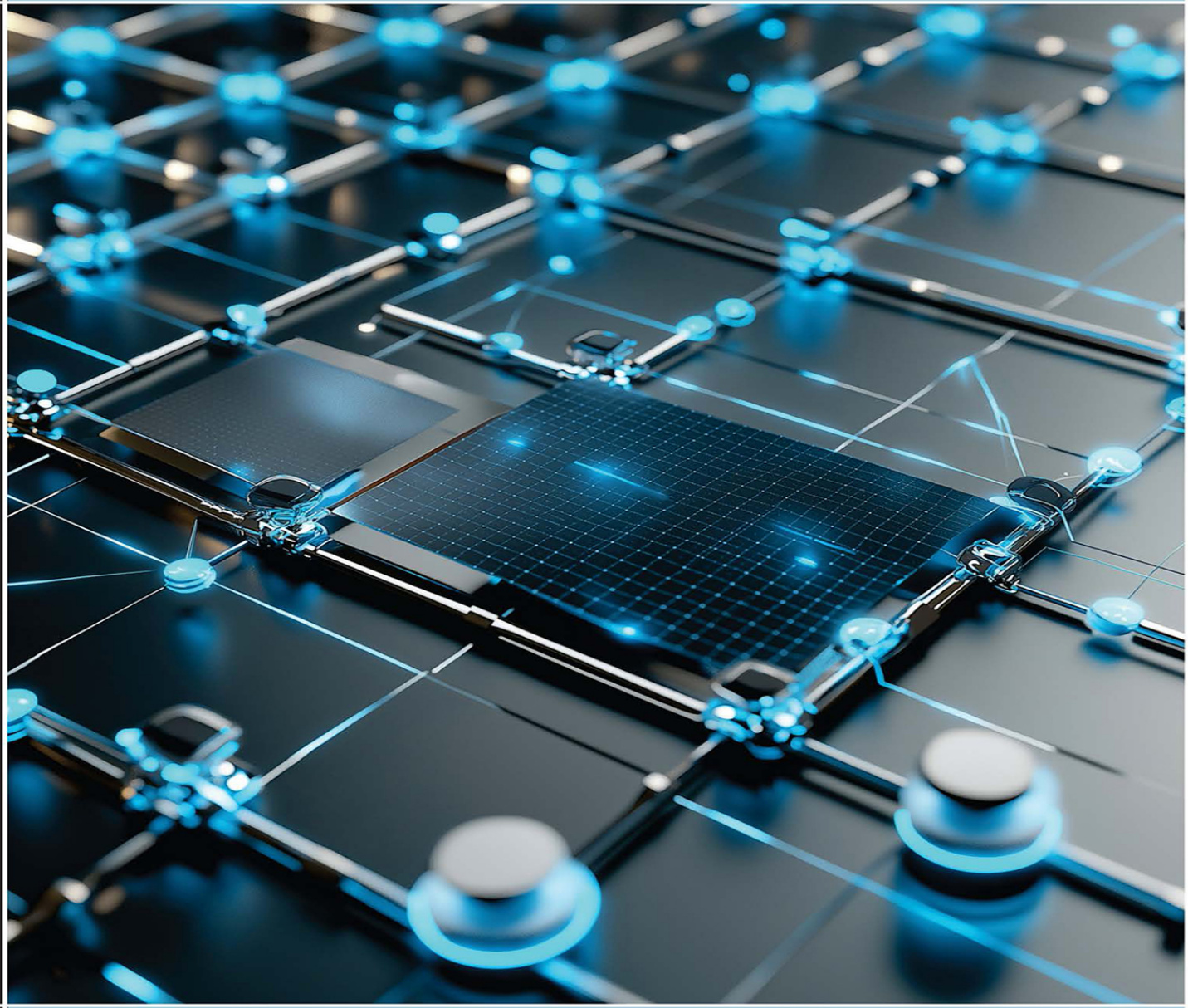

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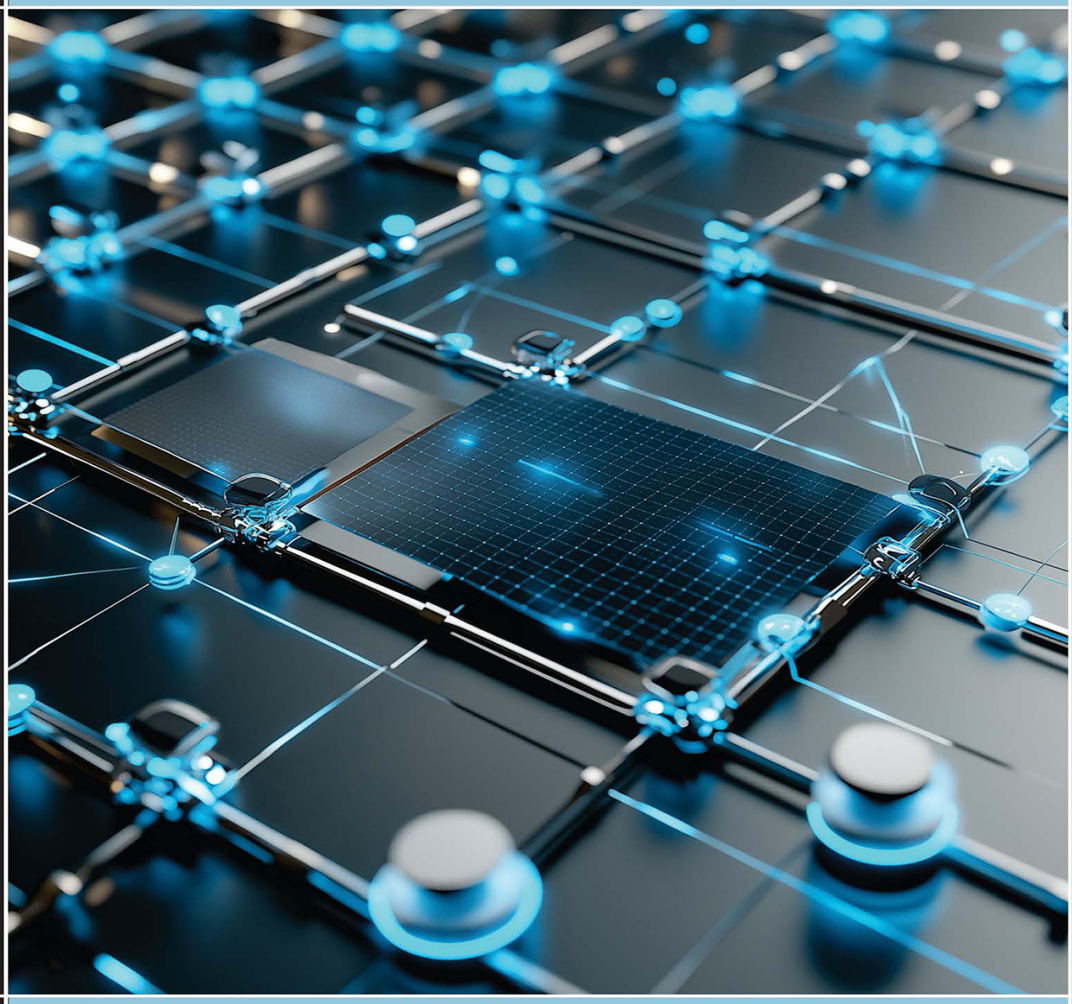

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Arpan Deyasi, PhD
Angsuman Sarkar, PhD
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Contents

Contributors

Preface

1. **A Structural Roadmap from Double Gate MOSFET to Junctionless Transistor: Comprehensive Review**
   Supratim Datta, Arpan Deyasi, and Angsuman Sarkar
2. **Design and Implementation of Fault-Tolerant Convolutional Neural Network for Safety-Critical Embedded Systems**
   Sowvik Dey, Arijit Patra, and Amiya Karmakar
3. **Impact of Electromagnetic Bandgap Structure Incorporated in Square Microstrip Patch Antenna**
   Pampa Debnath, Payal Poddar, Moitrayee Sardar, Jyotirupa Roy, Deyasini Ray, and Arpan Deyasi
4. **VLSI and Random S-box Based IoT Security by Variable Irreducible Polynomial GF (2^8) in Composite Field Arithmetic**
   Indrajit Das, Papiya Das, Papiya Debnath, and Subhrapratim Nath
5. **Recent Advances in Slotted Waveguide Antenna Design for its Use in Modern Microwave Remote Sensing**
   Mandar Chakrabarti, Malay Gangopadhyaya, and Abir Chattopadhyay
6. **Missing Cell Defect Analysis of Reversible 1-Bit Magnitude Comparator**
   Vaishali Dhare and Divy Modi
7. **Investigation of Optoelectronic Characteristics of Double Quantum Well Structure for Triangular Well Geometry**

Varsha Chowdhury, Nairwita Chakraborty, Reetangsee Dutta, Pampa Debnath, and Arpan Deyasi

8. **An Architecture for High-Gain Multistage CMOS Amplifiers: A Review**
   Caprio Mistry, Ria Bose, and Arighna Basak
9. **Analysis and Applications of MOSFETBased Memristor in Analog and Digital Circuit**
   Gouranga Mandal, Mourina Ghosh, and Pulak Mondal
10. **Characterization of GO, rGO, and PEI Doped Graphene Nanocomposites for Biosensor Applications**
    Hiranya Ranjan Thakur, Dhruba Jyoti Hazarika, Jiten Chandra Dutta, and Kabyashree Hazarika
11. **A Numerical Approach to Investigate the Effect of Work Function on the Important Cell Parameters of Heterojunction Solar Cell**
    Rewrewa Narzary, Geetartha Sarma, Satyajit Das, and Partha Pratim Sahu
12. **Design and Comparative Analysis of Different Geometric Structures of Micro-Cantilever Diaphragm for Biosensor Application**
    Geetartha Sarma, Jitendra Kumar, Barsha Barman, Bidyut Bikash Borah, Rewrewa Narzary, and Partha P. Sahu
13. **Design of a Sensitivity Improved Surface Plasmon Resonance (SPR) Sensor with Barium Titanate ($BaTiO_3$) and Blue Phosphorus-Tungsten Disulphide (BlueP-WS_2)/Black Phosphorous (BlackP) Hybrid Structure**
    Ritayan Kashyap, Udit Ranjan Baruah, and Biplob Mondal

Index

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Preface

The electrical and optoelectronic characteristics of semiconductor devices are significantly altered when compared with their bulk counterparts due to the device's decreasing dimensions. The realm of quantum electronics has now taken hold, and new features are being investigated from a variety of low-dimensional structures, opening the door to quantum information processing. Because new devices may be created, theoretical research in nanostructure has already demonstrated the enormous potential for improvement in the fields of electronics and photonics. Researchers and engineers use experimental methods or analytical/numerical techniques to tackle barriers and overcome difficulties.

The process of fabricating a device is extremely intricate and timeconsuming, and when the device's dimensions are at the nanoscale, extreme care must be taken before beginning work. This is because even little variations in the thickness of a layer or the composition of the material might result in the end-product having distinct electrical and optoelectronic characteristics. Therefore, correct computation taking into account the complicated band structure, composition of the heterostructure system, and more specifically the technique of computation is essential in order to prevent mistakes during the manufacturing of low-dimensional structures.

Numerous numerical techniques have been employed in the past to solve quantum well systems, with the finite element method (FEM) and finite domain time difference (FDTD) approach being the most optimal solution to date. The book's clear treatment of several intricate theoretical and analytical models for resolving issues with diverse nanodevices would be very beneficial for graduate students, researchers, and academicians.

Furthermore, this cutting-edge book on nanoelectronics covers the topic from several perspectives. The computing and telecommunication industries stand to gain greatly from the discoveries made here, as material composition and choice now determine the most important aspects of the performance of various low-dimensional devices.

Every chapter in this book starts with a strong theoretical foundation and covers the most popular topics in contemporary electrical engineering. The ongoing reduction in the size of devices, components, and systems necessitates advanced theoretical analysis that is backed by simulated results prior to real production. In order to create an interdisciplinary, all-encompassing technical product that addresses underlying physics, material aspects, structures in the nano-regime, and related end-products, that single objective is given maximum push within these two covers.

The nanoworld is incredible! Learning about it will prove both enjoyable as well as raise interest in finding solutions to the issues and struggles of many hardworking people in the actual world. One may practically enter the field of quantum electronics during the intriguing voyage documented in this curated book, and they should make an effort to familiarize themselves with it since each chapter keenly focuses on how it might assist humanity. Amazingly, the continuously changing aspects of nanoelectronics both create obstacles and offer means of overcoming them. This book will undoubtedly provide future engineers and researchers with valuable insights, which is where the success of producing this product—which will only serve to advance civilization over the next ten years—lies.

CHAPTER 1

A Structural Roadmap from Double Gate MOSFET to Junctionless Transistor: Comprehensive Review

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ABSTRACT

This chapter deals with comprehensive review on various kinds of junctionless transistors for potential applications in sub-micron and nanoelectronic circuits and systems. The journey starts from simple double gate structure to DG FinFET and later moves toward junctionless architecture. Among various structural variations: SOI, bulk planar configuration, double gate, tri-gate, and Tunnel FET are vividly discussed with a flavor on basic conduction mechanism. Detailed literature review is carried out for each specific type emphasizing chronological development of the devices, and therefore, improvement in electronic performance in each subsequent variation is also reported. This summative brief discussion

carries the essence of device architectural modifications for future possible techno-commercial applications.

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1.1 INTRODUCTION

For decades, one of the main disadvantages is CMOS scaling in the semiconductor industry. The aim of this downscaling is to increase the speed and capacity of the device. Over the years, multiple novel technologies have been proposed [1, 2 and 3], where the major focus area, or may be coined as one of the leading aspects is replacement of conventional bulk MOSFET technology by quantum transport based architectures, which are responsible for the growth of the semiconductor industry proposed by Moore's law [4]. Nowadays CMOS technology has grown exponentially to the 45 nm regime [5 and 6], the further use of CMOS technology is dominant in the near future, while further scaling beyond 45 nm of CMOS device [4, 5 and 6] is suffering tremendous challenges. Thus, during this limit, many effects have arrived in the junction which are namely (i) short channel effect is found in the device which includes threshold voltage roll off [7], (ii) subthreshold slope degradation and strong drain induced barrier lowering (DIBL) effect [8], (iii) quantum mechanical tunneling effect will observe direct band to band tunneling current between source and drain and gate oxide tunneling leakage current which flows through gate oxide insulator [9], and (iv) threshold voltage variation is obtained from device to device due to random doping concentration [10]. High leakage current found in the device during these effects, indicates the factors responsible for CMOS scaling [11, 12 and 13].

In order to nullify the short-channel effects, researchers developed multiple complex architectures [14, 15 and 16] as well as invoke novel material compositions [17, 18 and 19], with primary objective to enhance ON-to-OFF current ratio. Due to their better gain control, dual gate FETs have already demonstrated their significant efficacy in the RF mixer and amplifier application areas [20 and 21]. Despite its widespread use in sub-50 nm technology, 100 nm gate lengths are typically used for accounting due to fabrication challenges. Even though undoped DGMOSFETs have been reported numerous times [22 and 23], moderate doping may be taken into consideration for successful outcomes given its practical limitations.

Tri-gate structure [24], quantum wire FET [25], CNTFET [26], and single electron transistors [27] are also investigated in the last decade where subthreshold swing is set to be closer to the ideal limit, DIBL is substantially controlled, and transconductance is increased. In the next section, a brief literature review of double gate MOSFET is carried out.

1.2 LITERATURE REVIEW ON DOUBLE GATE MOSFET

The alternative structures are proposed beyond the 45 nm technology to avoid these effects, namely surrounding gate [28], Pi-Gate [29], Omega-Gate [30], tri-gate [31], and double-gate MOSFETs, which replaced bulk MOSFETs structure. Multi-Gate MOSFETs show better scalability and analytical simulation over bulk-MOSFETs [32]. The advantage of better scalability of multi-gate MOSFET is that it operates in shorter gate length at off state current condition; thus, power dissipation is increased in the device. DG MOSFET structure is very useful in device fabrication because it is highly suitable in designing process with conventional technology.

Figure 1.1 represents two different structures of DG MOSFET: firstly, the symmetric DG MOSFET which has identical gate work functions and secondly, the asymmetric DG MOSFET with different work functions is

illustrated in two gates. The main benefit of DG MOSFETs is that its body is usually lightly doped which is helpful during device fabrication.

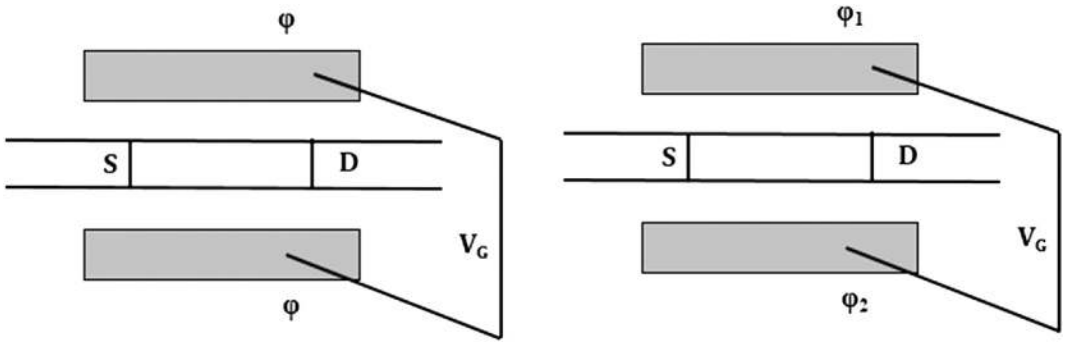

FIGURE 1.1 Schematic view of symmetric DG and asymmetric DG MOSFET.

The DG MOSFETs basically operate in two modes: three terminal and four terminal modes. In three terminal mode, the two gates in MOSFET structure are electrically connected and they are operated simultaneously as shown in Figure 1.2. When MOSFET is operated in four terminal mode, the biasing conditions are different for two gates. The advantages of four terminal driven mode are that it enables the circuit design in large space and the adjustment of threshold voltage in circuit design [33]. When MOSFET is working in four terminal driven mode and applies the fixed second gate voltage, it exhibits non ideal relationship in subthreshold slope. As a result, if the potential across the non-switching gate is fixed, than the potential of silicon film is insufficient and movement is restricted with the switching gate. The four terminal driven DG MOSFET produces less short channel effect than the three terminal DG MOSFET [34, 35 and 36].

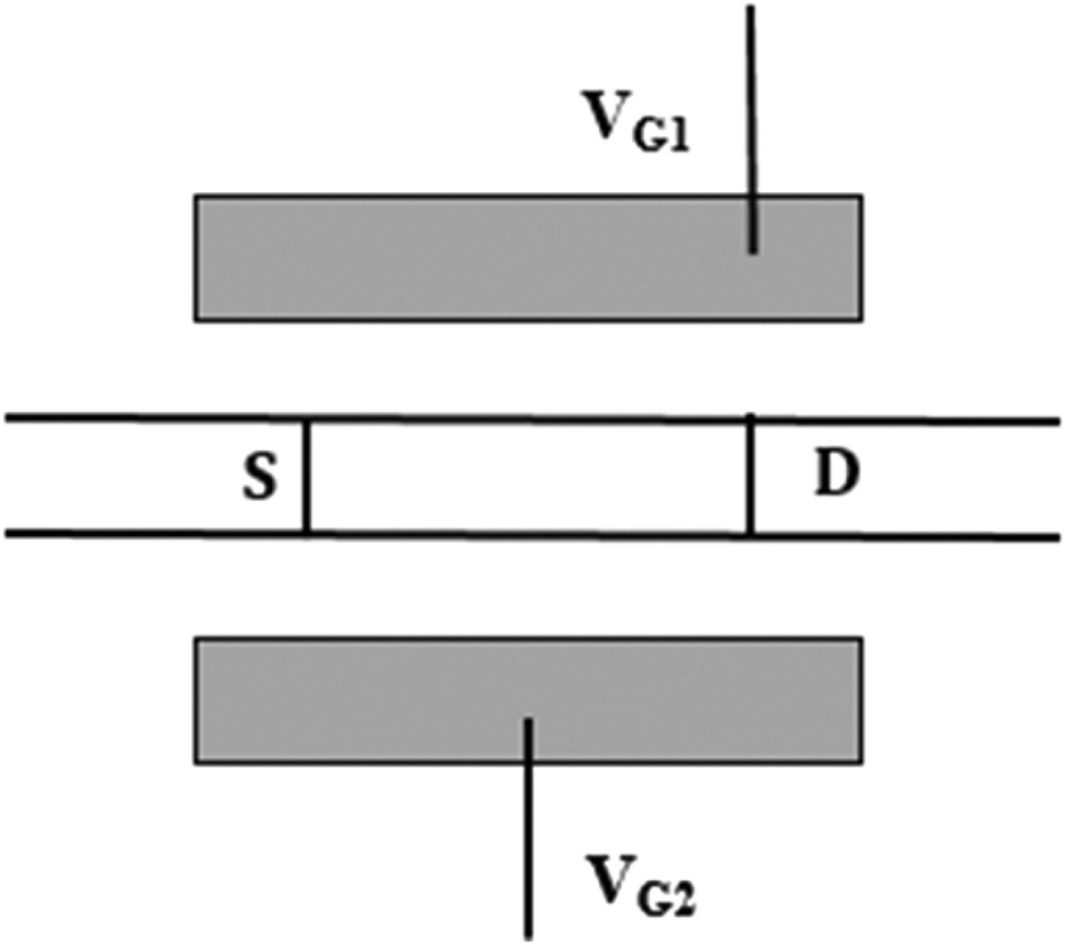

FIGURE 1.2 The device structure of a four-terminal driven DG MOSFET.

The construction of DG MOSFET is made using two gates structure and an undoped thin silicon film, resulting in better performance than conventional MOS. The advantages of DG MOSFET are that it produces better short channel effect, eliminates random doping concentration effect, and also carries better flow transportation in the device. These are the advantages of DG MOSFET over bulk MOSFETs.

Nowadays VLSI technology approaches its limitations, thus when CMOS device is scaled down, there are three primary device structures that are found which are namely DG MOSFETs, conventional bulk MOSFETs, and silicon-on-insulator (SOI) MOSFETs. Short channel effect is one of the

major effects that arise in the device when MOSFETs are further scaling down. For fully depleted SOI MOSFETs, the large variations in channel electrostatic potential are caused by the electric field at the drain region that goes through the buried oxide layer into the channel. But for the bulk and DG MOSFETs, the conducting surface pushes the electric field away from the channel region, thus bulk and DG MOSFETs display better behavior in short channel effect than in fully depleted SOI MOSFETs. Minimum channel length for fully depleted SOI MOSFETs due to short channel effect is represented by the following equations [37]:

$$L_{\min} = 4.5\left(t_{si} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox}\right) \tag{1.1}$$

For considering bulk MOSFETs, the minimum channel length can be given as:

$$L_{\min} = 2\left(W_d + \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox}\right) \tag{1.2}$$

Where W_d represents depletion width in bulk MOSFETs, also assuming that W_d is of same magnitude as t_{si}. Thus, short channel effect will be considered when further scaling is performed in bulk MOSFETs than fully depleted SOI MOSFETs. From the minimum channel length equation for bulk MOSFETs, it is seen that in order to scale down the device, both W_d and t_{ox} are reduced. Consequently, a higher doping concentration in the substrate is found when the depletion width in the device decreases. A higher concentration value in the substrate results in an increase in the direct band to band tunneling current, a decrease in carrier mobility, an increase in the capacitive effect at the junction, and a lower value of the subthreshold slope. Because of its undoped thin silicon body, the DG

MOSFET exhibits minimal band-to-band tunneling current, better subthreshold slope, and better control over the short channel effect. From a practical standpoint, it can be assumed that, given the same channel length, DG MOSFETs can exhibit better on/off current ratios than traditional bulk MOSFETs [38].

The tight coupling that occurs between the two gates of the DG MOSFETs results in a better subthreshold slope. Together with the voltage at the gate terminal, the potential across the silicon film is pushed away to the junction in the subthreshold region during the volume inversion stage. Therefore, in the case of long channel DG MOSFETs, the ideal subthreshold slope is found [35, 36, 37 and 38]. Leakage current in the device is reduced as a result of this controllable subthreshold slope, allowing for quick switching while the device is off. Additionally, a steeper subthreshold slope may allow the device to operate at a lower threshold voltage, resulting in a larger driven current that maintains the same on/off current ratio at the device.

Because DG MOSFETs have a lightly doped silicon body, the capacitance at the source and drain junctions is significantly reduced. Bulk MOSFETs have a significant amount of junction capacitance in the output capacitance region [39]. Therefore, by lowering the junction capacitances, DG MOSFETs achieve better switching speed results. The undoped body in DG MOSFETs slightly enhances the random dopant fluctuations. The number of dopants in the depletion region is usually smaller, typically in the range of 1000 dopants, when CMOS is further scaled down. The dopant totals are equal to the deviation of the square root of the total dopants [40]. This deviation gets stronger when the scaling factor is added to the depletion region, which causes the device's threshold voltage variation to change significantly. The control of gate work function over the threshold

voltage results in a significant reduction of doping fluctuation in undoped DG MOLSFETs.

The lack of depletion charges in DG MOSFETs causes the carrier mobility to increase quickly. The enhancement of carrier mobility in DG MOSFETs can be explained in two ways: first, by decreasing the impact of ionized dopant coulomb scattering, which increases carrier mobility; second, by greatly reducing surface roughness scattering caused by a lower electric field on the surface.

There are, in theory, three distinct DG MOSFET architectures. Bulk MOSFETs' plane structure is represented by Type I. The uniform doping of silicon channel thickness throughout the channel is facilitated by thin film deposition. Because of the fabrication process, which permits a bottom gate structure that is self-aligned with the top gate, a large number of parasitic capacitances occur in the source and drain region [41]. Because of this misalignment, a large gate delay is therefore suggested. As a result, it is challenging to enter the bottom gate region. The Type II structure presents a challenge to fabricating vertical source and drain configuration using current planar technology. Type III, which has two readily accessible, self-aligning gates, has the simplest fabrication process. Two variations of the Type III structure, DG FinFET and tri-gate MOSFET, are observed [42]. A DG MOSFET structure is created if both gate structures conduct current concurrently and the height of the silicon film is greater than the width. However, the structure is referred to as a tri-gate MOSFET when the height of the film structure is equal to the width and only the top gate permits current to flow through the junction. tri-gate MOSFETs' top gates aid in conducting current flow, which makes it easier for these gates to produce the short channel effect. Therefore, compared to FinFETs, the short channel

effect in tri-gate MOSFETs with thin silicon film thickness is more valuable [43].

Long silicon channels, which are in charge of raising the device's drive current, provide the device structure for both FinFETs and tri-gate MOSFETs. However, if the device is made of a tall vertical channel with appropriate uniform control, fabrication becomes challenging. As a result, drive current in the device is constrained by the channel's limited height, which lowers the layout structure of tri-gate MOSFETs' efficiency [44]. One of the better ways to raise the effective width value is to increase the drive current. Nevertheless, the device's total drive current separates and becomes an integer multiple of the total current value, leading to some unfavorable outcomes during the design and fabrication stages [45].

The sidewall structure of FinFET and tri-gate MOSFETs differs from the surface of bulk MOSFETs in terms of crystallographic orientation. Where the carriers in bulk MOSFETs move in the <100> direction, those in FinFET and tri-gate MOSFETs are located in the crystal pane in the <110> direction. From an experimental perspective, it is discovered that when the direction of carriers is changed in the 100> orientations, the hole mobility increases by 100% while the electron mobility in the 110> direction decreases by 8% in response to a high electric field [46]. The benefits of increasing hole mobility include improving the device's switching speed by speeding up CMOS.

Since the DG MOSFET's structure was first created [47], the manufacturers have made significant technological advancements. But when DG MOSFETs become the cutting edge of technology, new kinds of difficulties arise which include: one of the primary innovations is the inclusion of strained silicon in the structure of DG MOSFETs, which raises the region between the source and drain due to halo doping concentration.

The metal gate work function generates a set of threshold voltages and uniformly controls the channel. These days, strained silicon technology, halo doping, and high-k gate dielectrics are proposed in the structure of tri-gate MOSFETs [48]. This tri-gate MOSFETs structure aims to reduce the off current by 50% and increase the drive current by approximately 45%.

1.3 RESEARCH OUTLINE OF MODELING DG MOSFETS

The bulk MOSFETs architecture designing has shown different types of important characteristics; also long channel core model should be included in it. The features in an ideal core model of bulk MOSFETs are continuous, symmetric, accurate and efficient. These features have the main aim of the modeling of DG MOSFETs.

Despite being a well-known device, the small modeling of DG MOSFETs has not gained much traction since its design and is still in its infancy. It is evident that earlier research has modeled a few of the DG MOSFETs' physical properties. For instance, in [49], a sub threshold swing model was developed for short channel DG MOSFETs. In [50, 51, 52 and 53], a concise modeling approach for threshold voltage in short channel DG MOSFETs was presented. The development of the quantum mechanical tunneling effect for DG MOSFETs was done in [54]. In addition to the physical phenomenon previously discussed, the drain current model of DG MOSFETs was also taken into consideration. The primary goal in creating the architecture of DG MOSFETs is to have two gates that function well in both upper threshold and subthreshold areas and are independently operated. But this model does not provide accuracy for a device parameter because its designing is not based on the exact parameters. For a reason, the terminal charge model and capacitive effect are not included in this model.

The aforementioned research makes it clear that the compact modeling of capacitance, terminal charges, and drain current was subpar, and that this

model has some issues that make it helpful for transient, DC, and AC analysis. We will close the gap for the analytical modeling of the DG MOSFETs' capacitances, terminal charges, and drain current in this chapter. Comparing these models to the MOS transistor model, all criteria will be met and highly precise output will be produced.

1.4 LITERATURE REVIEW ON JUNCTIONLESS MOSFET

One of the biggest responsibilities and problems faced by manufacturers of electronic gadgets is to create products that are lightweight, compact, and smart. Because of Moore's law, the semiconductor industry has evolved remarkably from single transistors to millions of transistors that can be readily designed into a single integrated circuit [55]. This law states that gadget speed and CPU power will double every two years [56]. Therefore, one of the main goals in industry that has improved productivity gains is MOSFET scaling. Therefore, the semiconductor industry would suffer from ongoing MOSFET size reduction due to the emergence of short channel effects (SCEs). These effects result in a reduction in gate controllability over the conducting channel, which raises the gate leakage current [57]. The device performance will be impacted by additional effects resulting from MOSFET scaling, such as DIBL by source and drain junction [58]. The multigate MOSFET structure has been presented as a solution to the problems with the totally depleted SOI FET and the standard planar bulk MOSFET technology [59]. Many designs for multi-gate devices, namely double-gate MOSFETs, FinFETs, trigate MOSFETs, silicon nanowire architectures, and so forth are presented, with one of the leading technologies in transistor scaling to its extreme limit [60]. The anticipated gate length for double-gate devices is 7 nm by 2018, but the international technology specifies the gate length for fully depleted silicon on insulator (FDSOI) technology at 10 nm by 2015 [61].

Because of its strong electrostatic connection between the gate electrode and the conducting route, resilience against short channel effects and high current driven capacity, multi-gate structures are highly helpful in design [62]. Trigate and Gate-all-around designs are seen to be among the most successful MOSFET applications because they offer superior channel potential control. The gate electrode is wrapped around the semiconductor device to create these formations [62]. Longer electrode walls at the gate terminal in the buried oxide (referred to as "μ-gate" and "Ω-gate") have recently been shown to increase the current conductivity of triple gate MOSFETs [63]. The purpose of these structures is to prevent the electric field from extending into the semiconductor body [64]. Compared to double gate and trigate MOSFETs, GAA MOSFETs have superior characteristics [65]. Since MOS transistors function at nanoscale dimensions, stronger doping density gradients for this junction have been suggested [66]. Ultrashallow source and drain regions in semiconductors are created with high doping values due to the diffusion law and the behavior of the doping concentration gradients; as a result, innovative doping techniques and ultra-fast annealing methods are developed in junction design. Because it eliminates these issues, the development of junctionless transistors is highly helpful these days [67]. The source (S), channel, and drain (D) regions of the junctionless transistor, each have a high, homogeneous, and uniform doping concentration. As so, the gadget is built in a brief period of time.

1.5 STRUCTURAL CLASSIFICATION OF JUNCTIONLESS TRANSISTORS

Numerous hypotheses of junctionless transistors (JLTs) based on Lilienfeld's original transistor design are covered in this chapter. Many benefits of JLT structures over traditional MOSFETs were put forth, as JLT allowed for deep source and drain region expansions during the

manufacturing process. Additionally, the implant annealing process is avoided because a gate dielectric stack material is created, which has the benefit of reduced heat budgets and adds flexibility to the metal in the device and the gate dielectric material [67]. Various multigate JLTs have been used to demonstrate the inclusion of bulk planar, double gate, trigate, and nanowire structures in the manufacturing process.

1.5.1 JUNCTIONLESS SOI TRANSISTOR

This device structure is made up of a thin device layer put on top of a buried oxide layer that is positioned on top of a bulk silicon layer. Thus, as shown in Figure 1.3, a metal layer and a dielectric thin stack layer (with the opposing work function present in both layers) are constructed. Because of the differences in the work functions of those layers, there is no conduction between the source and the drain under zero biasing conditions [68]. The junctionless SOI-FET may be viewed as an asymmetric double-gate MOSFET, where the front gate bias is fixed and the rear gate functions as a substrate. Additionally, the front gate alone determines how controllable a structure is. Because of the back gate's potential lack of controllability, the subthreshold current in this device is limited by the thickness of the back gate oxide. Therefore, front gate bias influences the sub-threshold slope value, which is lowest in the subthreshold zone. Front gate bias is highly beneficial because it prevents the depletion of mobile charge carriers in the subthreshold region caused by an increase in back gate bias. As a result, when the device is constructed at a short gate length, the subthreshold current properties are enhanced [69].

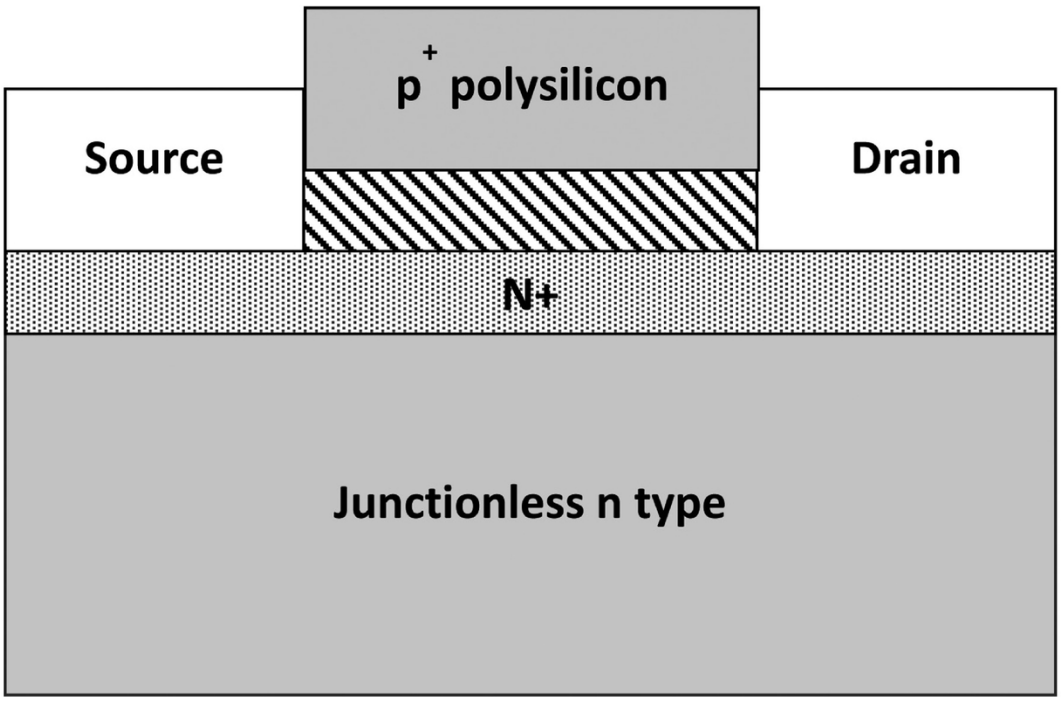

FIGURE 1.3 Schematic structure of SOI junctionless transistor.

1.5.2 BULK PLANAR JUNCTIONLESS TRANSISTOR

Because uniform doped ultra-thin SOI substrates show substantial scaling of SOI film thickness, they are costly to produce and present several technological obstacles. Bulk planar junction-less transistor (BPJLT), a source-drain-junction-less transistor, is suggested as a solution to these issues [69]. This device construction creates the connection by placing a thin n-type device layer on a p-type silicon substrate. As shown in Figure 1.4, gate dielectric is employed as a gate stack material and is produced on top of the n-type layer. In the BPJLT structure, junction isolation—rather than dielectric isolation—is the primary goal for the fabrication of devices. The doping concentration in the source, drain, and channel of this device is homogeneous and consistent. A thin dielectric layer that aids in separating from the channel is a component of both devices' construction, which uses a p-type gate metal. When the device is in the ON state, it operates in the flat band area, allowing leakage current to flow on the oxide layer. In the

OFF state, the device's volume is completely depleted [69]. The BPJLT has two benefits over the current JLT: it is more scalable and allows for additional controls through device parameter changes.

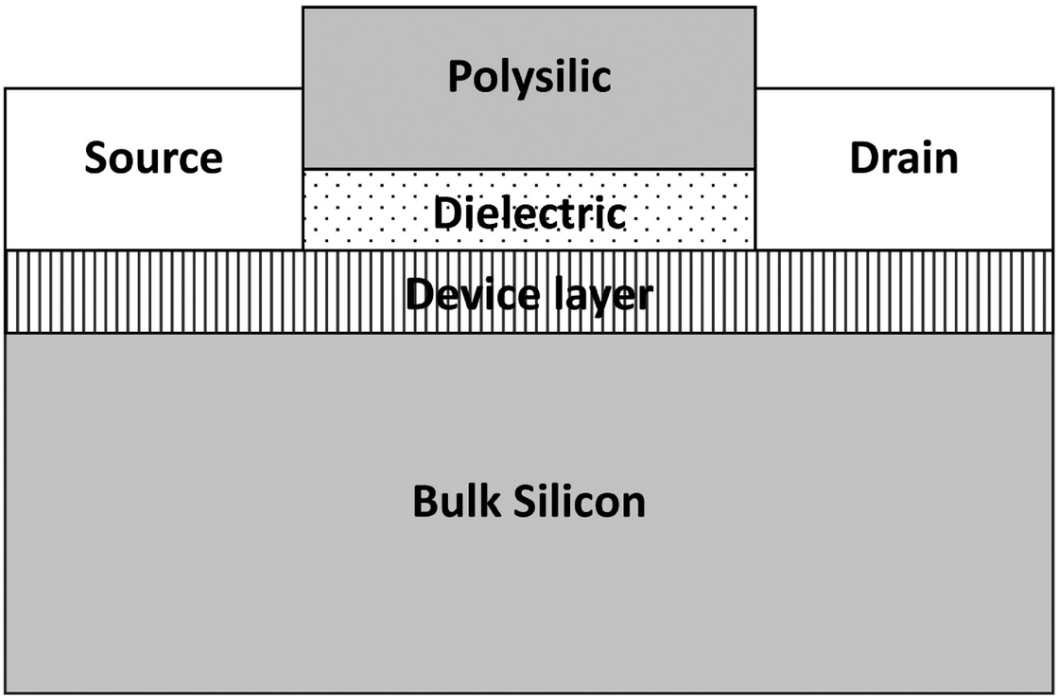

FIGURE 1.4 Cross sectional view of bulk planar junctionless transistor.

1.5.3 DOUBLE GATE JUNCTIONLESS TRANSISTOR

The conduction mechanism of a junctionless field-effect transistor (JLFET) is controlled by bulk current rather than surface mechanism; the channel is completely depleted when the device is in the off (OFF) state. Just like with a single gate, it is challenging to completely empty the channel during fabrication; hence, a suitable threshold voltage level is identified. Consequently, improved electrostatic control of the gate was made possible by a double-gate construction [70]. Two gates are used to create a junctionless double-gate MOSFET (JL-DGFET) construction; one gate is located at the top and the other at the bottom of the device.

The strongly doped thin silicon layer is sandwiched in between these two gates. These gates simultaneously switch on and off the device and oversee improving electrostatic control in the channel [70]. The totally depleted channel is found when the device is operated in the subthreshold region because the electric field at the gate area causes the bulk of charge carriers to flow away from the surface. When the device voltage reaches the threshold condition and the bulk current mechanism occurs in the junction, the neutral zone is in the middle of the channel. Maximum bulk current flows through the device and a neural channel is formed when the gate voltage rises over its value and reaches the flat band voltage [70]. For maximum level of gate voltage, the negative charges are composed in the surface layer of the channel, thus surface current flows in the junction. This structure provides small DIBL effect, high ON-OFF current ratio, simple fabrication process, and low device cost [71].

1.5.4 JUNCTIONLESS TRIGATE TRANSISTOR

As shown in Figure 1.5, the junctionless trigate structure has the gate wrapped around the substrate, which aids in improved conduction layer management. The channel is fully depleted when the majority of charge carriers are moved away from the junction by the electric field, resulting in a gate to channel capacitance that is high enough and has an adequate channel width. The gate to channel capacitance value will fluctuate in response to changes in the gate voltage. As a result, the top gate's effective width is increased and the device's threshold voltage is found to be sufficient. Band-to-band tunneling occurs as a result of further scaling the gate length which increases the OFF-state leakage current flowing through the device. An optimal subthreshold slope is found as a result of junctionless trigate MOSFETs' better performance at high temperatures. Better electrostatic control also results in a rise in the ION/IOFF ratio

across the channel [72]. The JLT device's majority charge carriers flow readily over the silicon film's enormous surface area; but, because the MOSFET is junction-based, the minority carriers are dispersed between the gate oxide contact and the film [73]. As a result, the JLT device has greater mobility below the flat band voltage level and has improved back biasing efficiency. But since bulk conduction is decreased in thin JLT devices and gate control is seen sideways in the junction, the back bias impact is minimal [73].

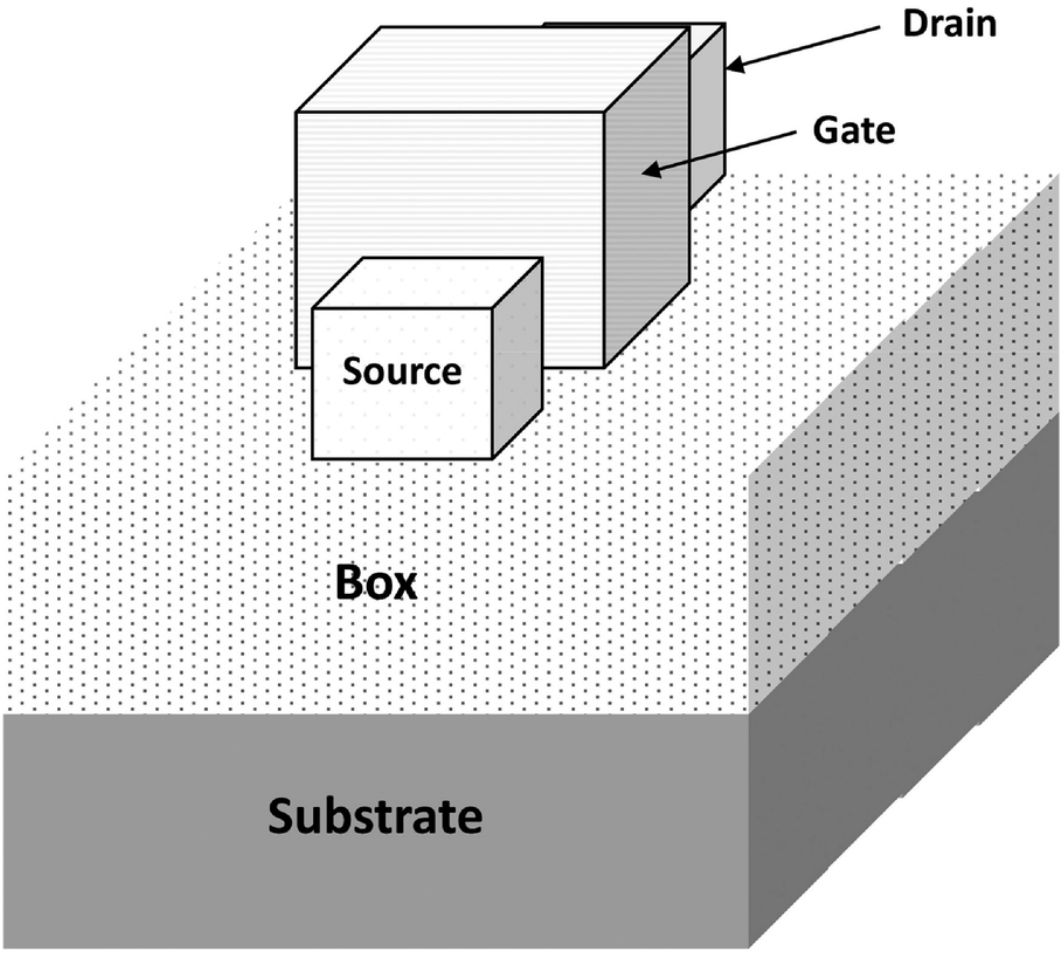

FIGURE 1.5 Cross-sectional view of junctionless trigate transistor.

1.5.5 JUNCTIONLESS NANOWIRE TRANSISTOR

In multigate nanowire transistors, the gate electrode has improved response for channel control and prevents short-channel effects [74]. Since the source and drain regions have extremely steep doping gradients, aggressive scaling down of the devices has several drawbacks, including a severely constrained junction base nanowire transistor structure. In order to get around these problems, a novel transistor design known as the junctionless nanowire transistor (JNT) was developed [74].

Thin semiconductor layers make up JNT, as shown in Figure 1.6. The narrow device construction aids in depleting full charge carriers while the device is in the OFF state. Due to its high doping, this device has a high ON-state current flow. The JNT device mechanism differs from the structure of traditional multigate FETs. Under the threshold voltage, a highly doped nanowire in this structure generates a large electric field that flows perpendicular to the current flow; however, above the threshold, this electric field becomes zero, resulting in the discovery of an electrically neutral conducting channel. However, when the MOSFET is turned on, the conducting path experiences the highest electric field value in the inversion-mode (IM) and accumulation mode (AM) [75].

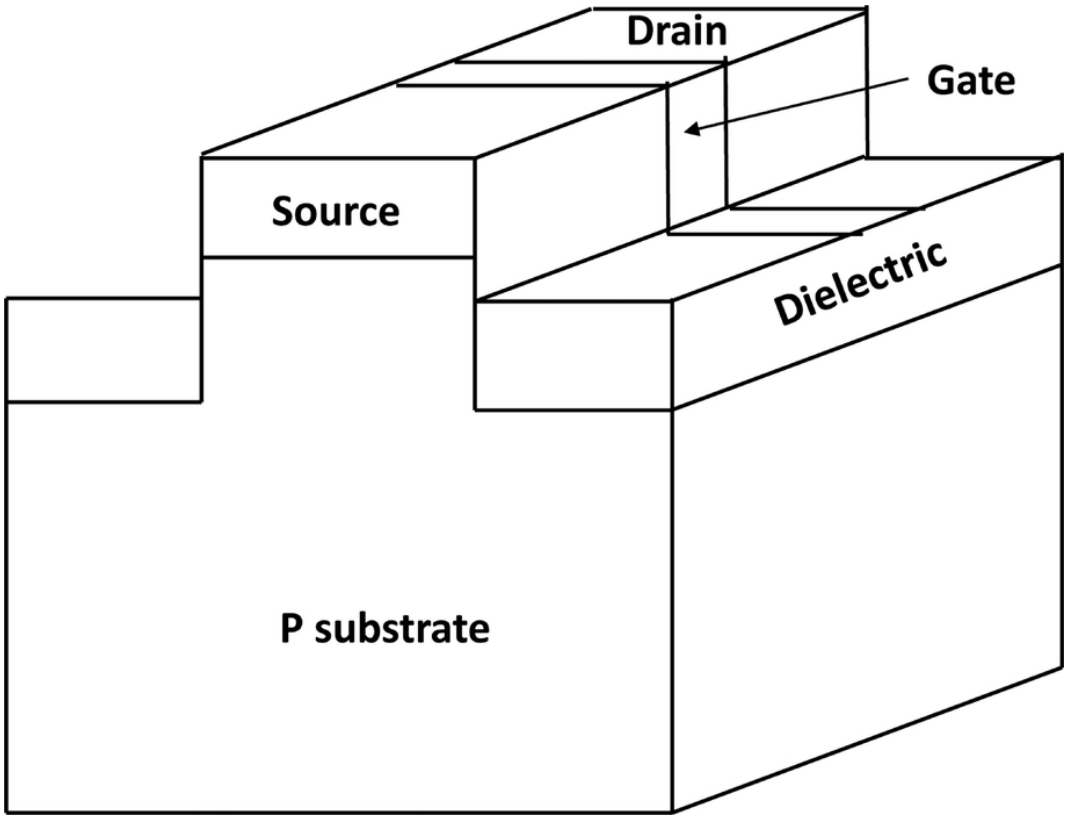

FIGURE 1.6 Junctionless nanowire transistor.

1.5.6 JUNCTIONLESS TUNNEL FET

Although the JLFET construction has several limitations due to its subthreshold slope (SS), it offers better electrical properties and less process variability than the standard MOSFET structure. Junctionless tunnel FET construction [76] with low power has lower SS, lower ON state current, reduced energy consumption, and lower operating voltage.

The operation of this apparatus is based on the band-to-band tunneling (BTBT) principle. This device contains a gated p-i-n diode, which, as shown in Figure 1.7, is reverse biased when the gate is stretched across the intrinsic area. This device's valence band and conduction band overlap as well as the barrier in the tunnel junction, which shows the junction's ON and OFF state conditions [77]. In the ON state condition, lower leakage

current flows in this device, thus higher I_{ON} and I_{OFF} ratio is obtained also provided steeper SS.

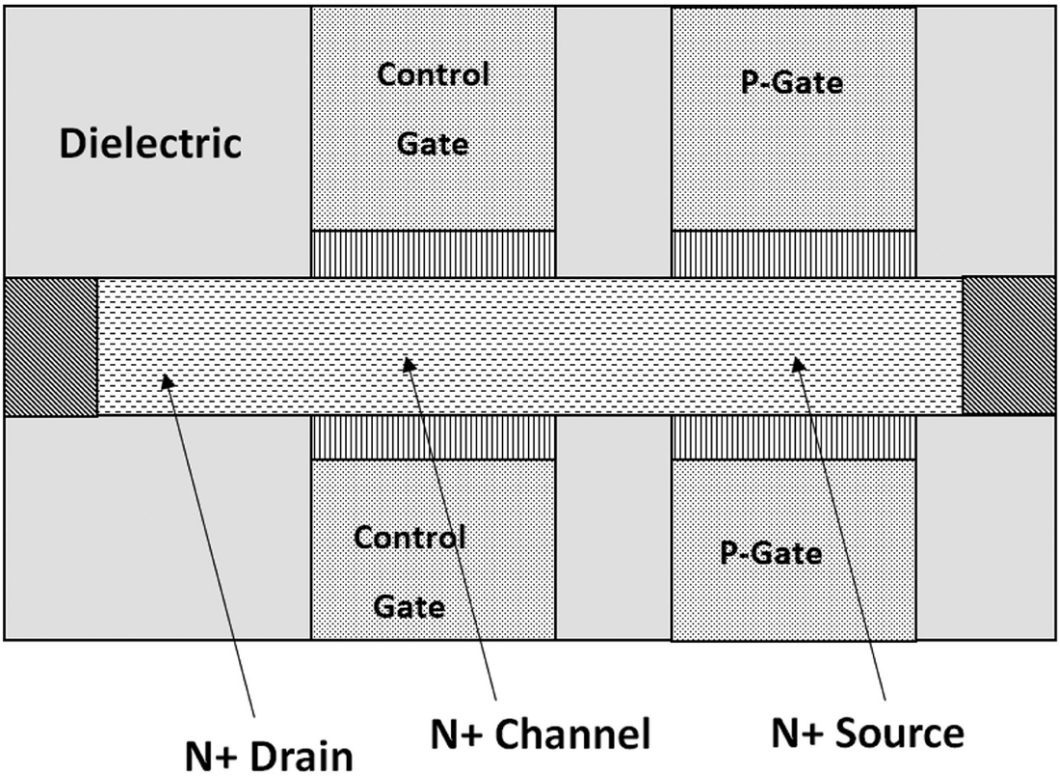

FIGURE 1.7 Junctionless tunnel FET.

1.6 CONCLUSION

This chapter describes the structural variation of junctionless architecture, in a nutshell, in connection with earlier double-gate MOSFET. Extensive literature is being studied to determine the chronological development, and pros and cons of each stage are noticed while developing further complex designs. Several structural variations are covered in detail, with a focus on fundamental conduction mechanisms, including SOI, bulk planar configuration, double gate, tri-gate, and tunnel FET. For every particular type, a thorough literature review is conducted with an emphasis on the devices' chronological development. As a result, advancements in electronic performance in each later version are also documented. The

essence of device architectural modifications for potential future techno-commercial applications is conveyed in this succinct summary discussion.

KEYWORDS

- **double-gate MOSFET**
- **finFET**
- **junctionless transistor**
- **nanowire transistor**
- **quantum mechanical tunneling effect**
- **SOI transistor**
- **short channel effect**

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CHAPTER 2

Design and Implementation of Fault-Tolerant Convolutional Neural Network for Safety-Critical Embedded Systems

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ABSTRACT

Convolutional neural networks (CNNs) have gained significant attention in safety-critical embedded systems, such as those deployed in autonomous vehicles, medical devices, and industrial control systems, for their remarkable capabilities in image and pattern recognition tasks. In addition, the fault-tolerance capability is also appreciable. This chapter proposes a fault-tolerant approach for implementing CNNs on field-programmable gate arrays (FPGAs) to enhance the reliability and robustness of the embedded system. The fault injection mechanism is also applied to create a faulty

environment, yielding reduced effort for testing the system's fault tolerance mechanism. A comprehensive analysis of memory-fault sources and their impact on CNN-based systems has been discussed. Experimental results demonstrate that the fault-tolerant approach effectively corrects faulty output, enhancing the reliability and robustness of CNN-based embedded systems. Additionally, this chapter investigates the trade-offs between fault tolerance and resource utilization in the FPGA implementation.

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2.1 INTRODUCTION

In recent years, convolutional neural networks (CNNs) have demonstrated unparalleled performance in a wide range of computer vision tasks, revolutionizing industries such as autonomous driving, medical imaging, and industrial automation. As these safety-critical embedded systems continue to pervade various domains, ensuring their reliability becomes paramount [1]. However, in safety-critical applications, single points of failure and unpredictable operational environments pose significant challenges to conventional CNN implementations.

In this section, a thorough literature review has been done on (a) binarized neural network (BNN), (b) deep neural network (DNN), (c) convolutional neural network (CNN), (d) fault injection techniques, and (e) fault tolerance. The following sections describe the details.

a. **Binarized neural network:** A BNN is a special type of neural network architecture that employs binary values for both input data and weights. In a BNN, the activations of neurons are binarized,

meaning they are set to either 0 or 1 based on certain thresholds [2]. This drastic reduction in the number of possible activation levels helps reduce memory requirements and computational complexity.

b. **Deep neural network:** DNNs have gained significant attention and popularity in recent years due to their remarkable ability to handle complex tasks, such as image and speech recognition, natural language processing (NLP), and decision-making in various domains. The depth of the network allows it to learn hierarchical representations of data, capturing intricate patterns and features at different levels of abstraction [3]. In a DNN, data are fed through the input layer and passes through multiple hidden layers, where each layer's neurons perform computations and progressively extract higher-level features from the input data [4]. The last layer is the output layer, which provides the final prediction or classification result. More number of hidden layers can solve more complex problems [1].

   Input layer: This layer accepts inputs in different formats provided by the programmer.

   Hidden layer: Hidden layer(s) are present in between the input and output layers. It calculates and finds hidden features of the input data.

   Output layer: After several transformations using hidden layers, it produces the output and is conveyed using this final layer.

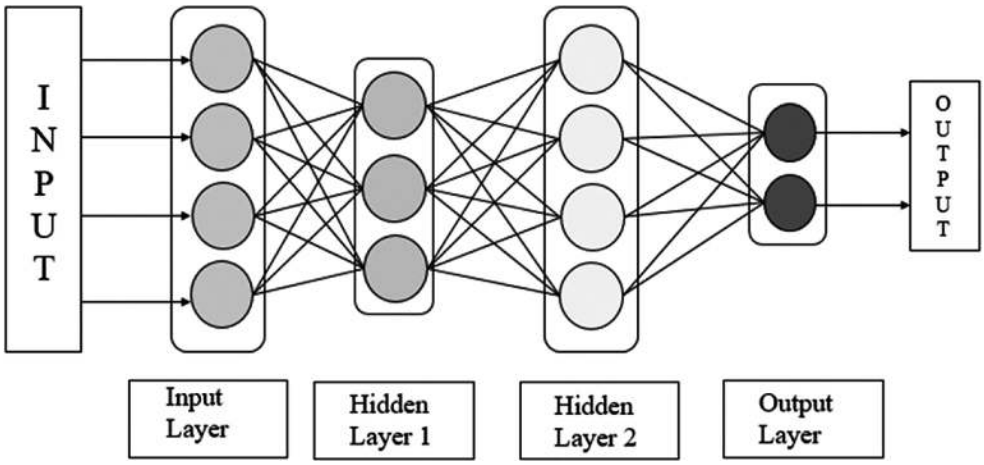

FIGURE 2.1 Deep neural network.

c. **Convolutional neural network:** A CNN is a kind of artificial neural network designed mainly for image processing. It is inspired by the animal visual system and is generally used in computer vision applications, such as image recognition, object detection, and image segmentation [1].

The key feature of a CNN is its ability to automatically learn hierarchical representations of visual features from the input data. This is achieved through the use of the convolutional layer, which applies filters (also identified as kernels) to the input image, capturing local patterns and features. These filters slide over the image, performing element-wise multiplications and summations, producing feature maps that emphasize different patterns [5].

To further enhance feature extraction, CNNs also incorporate pooling layers, which reduce the spatial dimensions of the feature maps while preserving important information. The max pooling operation is the most popular pooling method, which takes the highest value within a certain window.

The combination of convolutional and pooling layers allows CNNs to efficiently learn progressively complex features from low-level edges

and textures to high-level object representations [3]. The final layer of a CNN naturally consists of a fully connected layer and an output layer, which use the learned features to make predictions about the input image [5].

Due to their architecture, CNNs have demonstrated remarkable success in various computer vision tasks, achieving state-of-the-art results in image classification challenges like ImageNet and enabling breakthroughs in fields like autonomous vehicles, medical imaging, and more. Their ability to automatically learn relevant features from the environment without the requirement of hand-crafted features, represents them as an essential tool in modern AI applications [6].

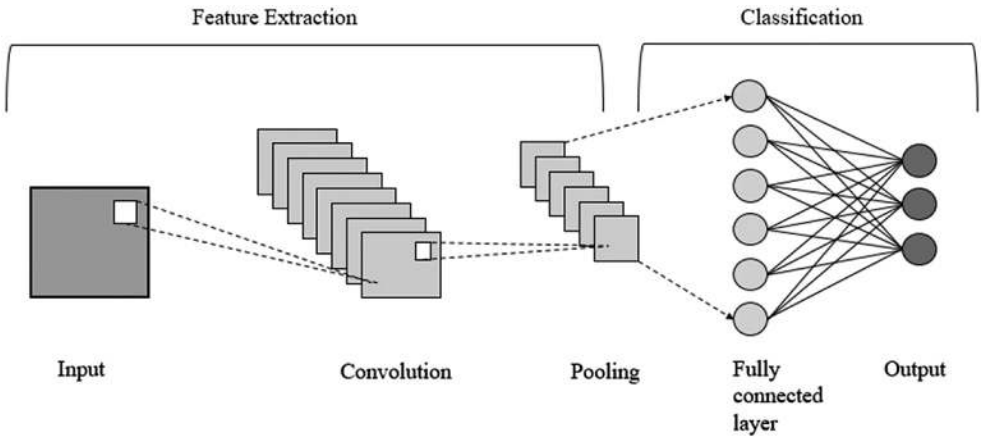

FIGURE 2.2 Convolutional neural network.

d. **Fault injection techniques:** Fault injection techniques are methods used in software and hardware testing to assess the resilience and reliability of a system. By intentionally introducing faults, such as errors, researchers and developers can identify vulnerabilities and weaknesses in the system's design. Some common fault injection techniques include:

- *Software-based fault injection (SWIFI):* This involves deliberately injecting faults into a software application's code or data to

observe how the system reacts. Examples include flipping bits in memory or modifying variables to simulate unexpected behaviors [7, 8].

- *Hardware-based fault injection (HWIFI):* This technique focuses on introducing faults directly into the hardware components of a system. Examples include manipulating power supply levels, inducing electromagnetic interference, or altering clock frequencies to observe how the hardware responds [7, 8].
- *Transient fault injection (TFI):* Introduces temporary or transient errors into the system. These errors may occur due to environmental factors, such as radiation or electromagnetic interference, and can lead to temporary malfunctions [7, 9].
- *Permanent fault injection (PFI):* Introduces permanent or long-lasting faults into the system. This can simulate scenarios where components degrade over time or are subjected to extreme conditions [9].
- *Fault injection testing tools:* Specialized tools and frameworks are used to automate and control the injection process. These tools help simulate various fault scenarios and measure the system's response [8].
- *Single event upset (SEU) injection:* Specifically targets memory elements by inducing bit flips or data corruption, often seen in radiation-induced errors [10].
- *Environmental fault injection:* This technique involves exposing the system to various environmental stressors, such as extreme temperatures, voltage fluctuations, or radiation, to evaluate its resilience under real-world conditions [11].

- *Circuit-level fault injection:* In hardware systems, this technique involves manipulating the electrical characteristics of circuit components to provoke faults [12].
- *Dynamic fault injection:* In the year of 2019, Dey et al. proposed a modern technique to inject a fault into the semiconductor memory system to moderate the effort of testing the fault-tolerant algorithms [13]. In this method, they proposed a random location selector to select a memory location randomly if the fault injector is enabled and injects a fault into that location to create the faulty environment.

MODIFI, LFI, DOCTOR, and so forth are the fault injection tools used in various sectors [14, 15].

e. **Fault tolerance:** Fault tolerance is a feature of the system that works properly in the event of a fault [16]. A fault-tolerant CNN is designed to maintain functionality and performance even in the presence of errors or faults. It employs techniques to handle various types of failures, such as hardware malfunctions, noise in data, or adversarial attacks. These techniques may include redundancy, error correction codes, dropout layers, and adaptive learning strategies. By integrating fault tolerance, CNNs can enhance robustness and reliability, making them more resilient in real-world scenarios where errors are likely to occur. Fault tolerance is necessary to ensure the continued operation and reliability of systems, especially in critical or high-stakes environments. It refers to a system's ability to continue functioning even in the presence of hardware failures, software errors, or other unexpected events [17]. Here are some reasons why fault tolerance is essential:

- *Reliability and availability:* Fault tolerance helps maintain system availability and reliability by minimizing downtime due to failures.
- *Cost of downtime:* Fault tolerance helps mitigate losses by reducing the impact of failures.
- *The complexity of modern systems:* Fault tolerance mechanisms help manage this complexity and ensure that a failure in one portion of a system doesn't clue to a complete system failure.
- *Hardware and software imperfections:* Fault tolerance strategies, such as redundancy and error detection/correction, help compensate for these imperfections and prevent them from causing catastrophic failures.
- *Critical applications:* Fault tolerance is crucial in such cases to ensure the safety of people and the environment.
- *Scalability:* Fault tolerance mechanisms can be designed to scale alongside the system, maintaining performance and reliability as the system grows.
- *Data integrity:* Fault tolerance measures, such as data replication and checksums ensure the integrity of data even in the presence of failures.

Overall, fault tolerance is necessary to ensure that systems can continue functioning even when faced with various types of failures. It helps prevent disruptions, reduce downtime, maintain reliability, and mitigate risks across a wide range of applications and industries. There are many ways to tolerate the fault—either using by-passing modes or by prediction of the data.

In this chapter, the fault-tolerant mechanism for binarized CNN has been discussed. Some previous work related to fault-tolerant BCNN has been illustrated in the next section. The proposed mechanism with its working

principle has been described in section III followed by the design implementation section and results analysis section. This chapter is concluded by discussing its achievements and future work as described in the conclusion section.

2.2 RELATED WORKS ON BINARIZED CNN

A neural network mimics the working principle of a biological brain. The CNN is mainly concerned with four types of neural layers. Firstly, the main fundamental block of a CNN is the convolutional Layer [5]. In this layer, the input image matrix is convolved with the kernel matrix also known as the mask. This layer is followed by the activation layer. An activation function (linear or non-linear) is used. In CNN, mostly non-linear ReLU activation function is used [4]. Using this activation function, some unwanted data are filtered out. To converge the data for the final layer, the amount of data should be reduced. This job is done after the activation layer, called the pooling layer. There may be several pooling layers present in the model according to the requirement of the system. The final layer called the fully connected layer collects several pooled data using different kernels. After this layer, the feature of the input pattern can be determined. A detailed overview of a CNN is described as follows:

1. Convolutional layer: A convolutional layer is a fundamental building block in CNNs, a class of deep learning models primarily used for tasks involving structured grid-like data, such as images [6]. Convolutional layers are designed to automatically and adaptively learn spatial hierarchies of features from input data.

   The key concept behind convolutional layers is the convolution operation (C), which involves sliding a small filter (also called a kernel (K)) over the input data (e.g., an image (X)) and computing dot

products between the filter's weights and the corresponding pixel values in the input. This process results in the generation of feature maps that capture various patterns and features within the input data. The size of the kernel is a perfect square matrix of 3 × 3 or 5 × 5 pixels. The operation is a linear one and is formulated as: @@ j are row and column indexes, respectively.

2. ReLU layer: The rectified linear unit (ReLU) activation function is mostly used in CNNs. It introduces non-linearity to the network, allowing it to learn complex relationships in the data [2]. The ReLU activation function is defined as follows:

$$\mathrm{ReLU}(\mathrm{x}) = \max(0, \mathrm{x})$$

In the context of a CNN, the ReLU layer is applied element-wise to the output of a convolutional layer or a fully connected layer. It replaces all the negative values in the output with zero while keeping the positive values unchanged. Mathematically, this can be represented as:

$$\mathrm{Output} = \mathrm{ReLU}(\mathrm{Input}) = \max(0, \mathrm{Input})$$

The ReLU activation has become popular in CNNs due to its simplicity and effectiveness. It addresses the vanishing gradient problem and allows the network to learn faster and more efficiently. Moreover, ReLU's sparsity-inducing property (turning negative values to zero) can lead to more robust and sparse representations in the network.

3. Pooling layer: Pooling, in the context of CNNs, refers to a down-sampling operation that reduces the spatial dimensions (width and height) of a feature map while retaining important information [3]. Pooling helps in reducing the computational load and controlling

overfitting by extracting the most relevant features from the input data. There are two common types of pooling operations used in CNNs: max pooling and average pooling. In max pooling, a fixed-size window (typically 2 × 2 or 3 × 3) slides over the input feature map [6]. At each position of the window, the maximum value within the window is selected and used to represent that portion of the input in the pooled output. Average pooling is similar to max pooling, but instead of selecting the maximum value within the window, it calculates the average value of the elements in the window and uses that as the representative value for the pooled output.

4. Fully connected layer: In CNNs, a fully connected layer, also known as a dense layer, is a type of neural network layer that connects each neuron to every neuron in the previous layer. This is in contrast to convolutional and pooling layers, which have a local receptive field and shared weights [6]. In the context of CNNs, fully connected layers are often used at the end of the network to make predictions based on the features extracted by earlier convolutional and pooling layers [2]. These fully connected layers aggregate the learned features and make the final classification or regression decisions.

In this chapter, fault tolerance in binarized CNNs has been discussed. Therefore, most of the values including inputs (image and kernel), activation function, pooling, and fully-connected layers are binary. Only once, after the convolution operation, it contains multiple-bit binary data. This has been resolved in the next step, in the ReLU layer.

An example makes it easier to understand the functionality of the binarized convolution neural network (BCNN). Let an image of the English letter ‘X’ be taken as an input binary image. Figure 2.3 shows the representation of the input image. The resolution of the image is taken as 11

× 11 pixels with a double row of zero padding. This zero padding is needed for convolution operation. It depends on the size of the kernel. Here, the kernel matrix of 5 × 5 pixels has been taken. To determine the kernel matrices, the edge detection of the input image has been done. Figure 2.3 also explains how the kernels are selected. Different colors are used to justify separate kernel matrices. In this chapter, three different filter/kernel matrices have been used.

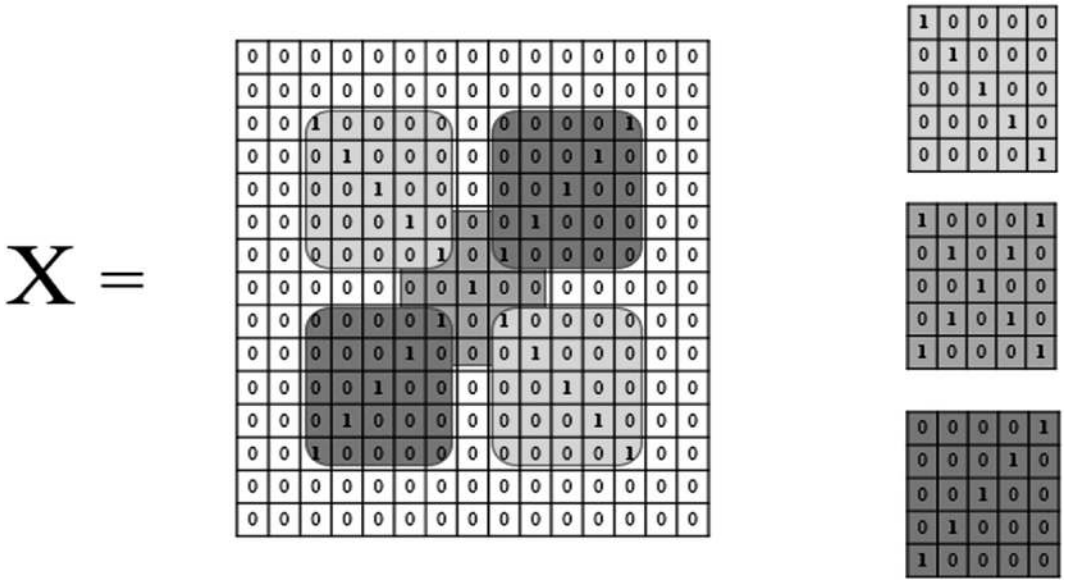

FIGURE 2.3 Input image matrix and its kernels. ⏎

Figure 2.4 describes each step involved in the BCNN and also ensures that the system does not contain any fault (non-faulty condition). One of the filter matrices has been taken as an example. This figure involves only the first three steps including convolution, ReLU, and pooling. The max pooling method is used in this chapter. When the first three steps using all three kernel matrices are completed, only then the fully connected layer can be determined. Figure 2.5 describes the fourth or final layer, the fully connected layer.

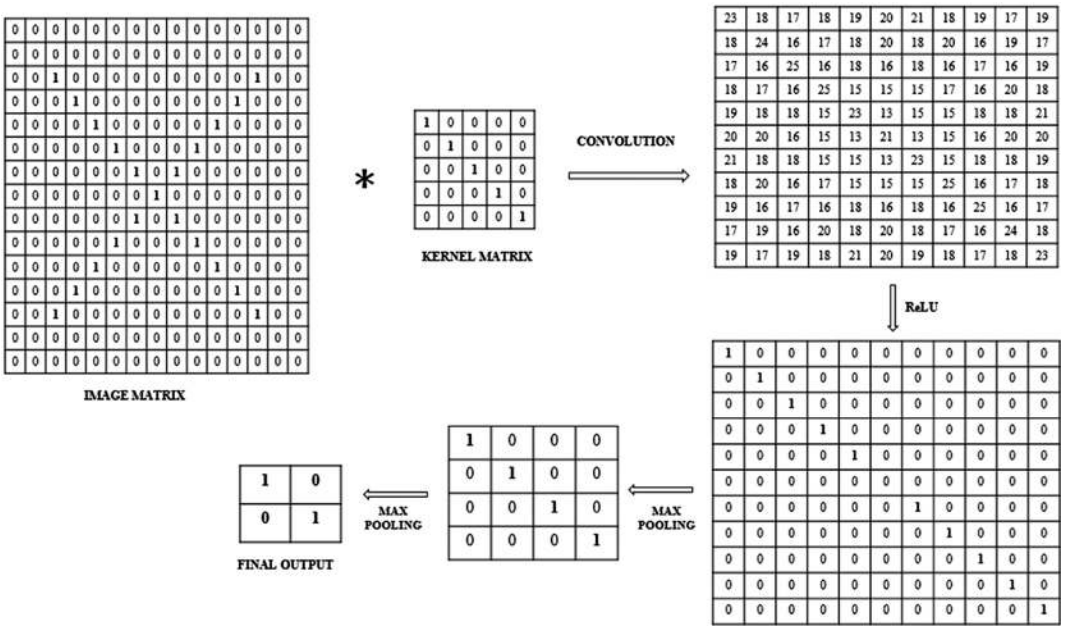

FIGURE 2.4 Non-faulty binarized convolution neural network steps.

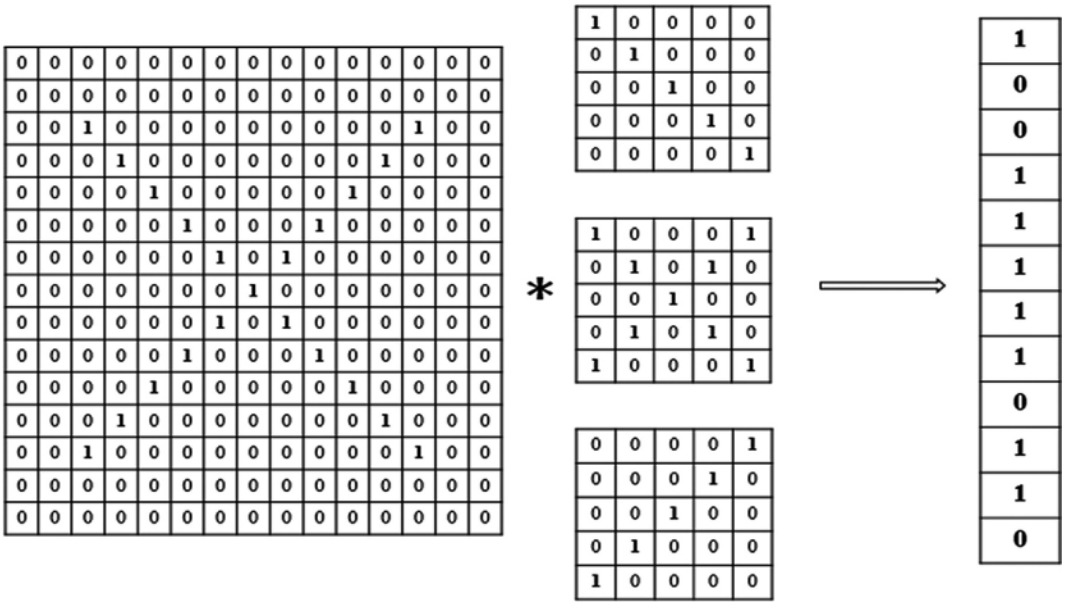

FIGURE 2.5 Output of fully connected layer of binarized convolution neural network (without fault).

This chapter mainly deals with the fault-tolerance mechanism of the BCNN. To determine the success of the fault-tolerant algorithm, the system must have a faulty condition. Dey et al. [2] have developed a fault injection

mechanism to create a faulty environment for BCNN [2]. A brief discussion of such fault injection mechanism will be done in this section.

A fault-injector model has already been developed for injecting the fault into the filter/kernel. The kernel matrices are nothing but the feature/edge of a given matrix. The main objective of the CNN is to determine the objective according to the given kernels. Therefore, the kernels are kept in the memory of the system previously. The semiconductor memory may fail to keep the kernels in it due to several causes of memory failure. This kind of faulty environment can be created by introducing the fault into the kernel.

Figure 2.6 describes the block diagram for the fault injection mechanism. The fault injector block is preprogrammed with one of the fault injection algorithms. An enable signal activates the block to invoke fault into the kernel. When the fault is incorporated into the system then the faulty output can be observed. Figure 2.7 describes the faulty changes in the output due to invoking the fault in the system.

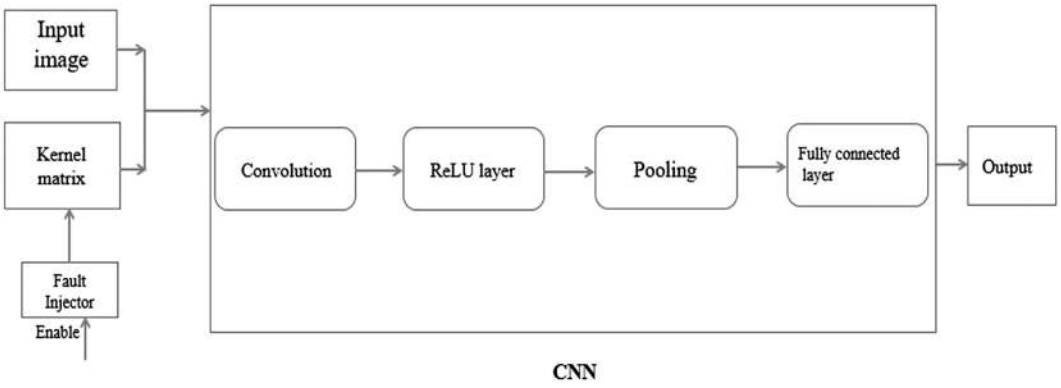

FIGURE 2.6 Fault injection mechanism in binanzed convolution neural network ⏎

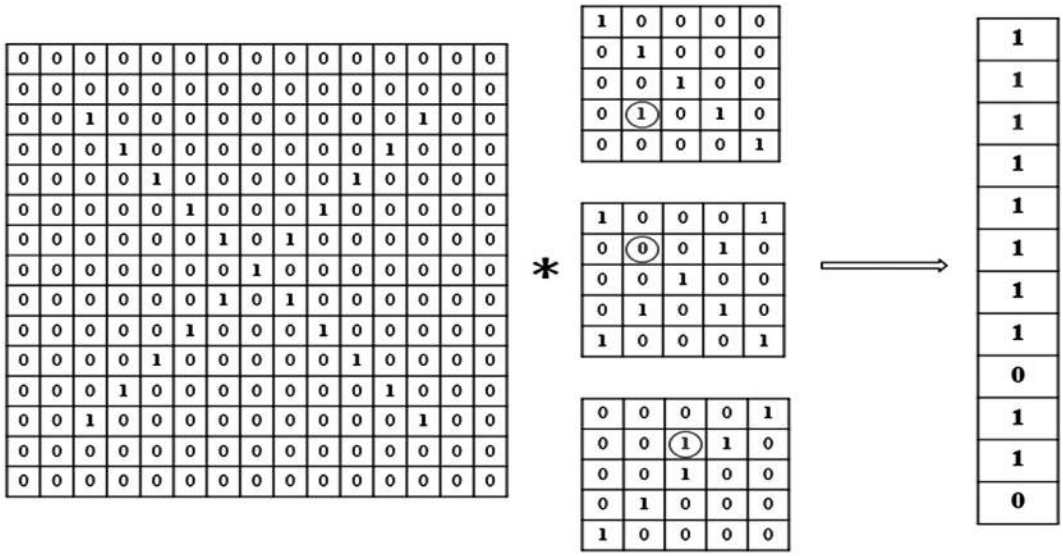

FIGURE 2.7 Fully connected output after fault injection in binanzed convolution neural network ⏎

Dey et al. [2] also summarized that the neural network itself is highly fault-tolerant. Therefore, after several experiments, their fault injector could invoke faults that reflected at most 33% error at the output of the fully connected layer [2].

2.3 PROPOSED METHODOLOGY

In this chapter, a fault-tolerant model for BCNN has been designed and implemented. Fault of a system can be tolerated either by bypassing the fault or by regenerating the missing data. In this chapter, the bypassing technique is used to make the system fault-tolerant. In the convolution layer, the bypassing technique has been incorporated. In this layer, before doing the convolution operation, a check has been made for faulty kernel data. If the kernel does not contain any faulty data (Z), then normal convolution operation has been done. But if a single-bit fault is there in the kernel, then the convolution operation is omitted only for that location. This can be formulated as follows:

$$C_{ij} = \Sigma\Sigma X_{ij} \times K_{ij}; //\forall i^{th} \text{ row and } j^{th} \text{ column and } K_{ij} \neq 1'bz.$$

Figure 2.8 describes the proposed fault-tolerant algorithm for BCNN which can bypass the faulty locations during the convolution operations.

```
Procedure_fault_tolerant_convolution (input matrix, kernel matrix)
set result = 0;
if kernel [i][j] l'bz;
then bypass for convolution operation for i,j position
else
result = result + input [i][j] "' kernel [i][j];
end if
end procedure
Procedure_fault_tolerant_BCNN(input matrix, kernel matrix)
a <= fault_tolerant_convolution (input matrix, kernel matrix);
b <= relu (a);
c <= maxpooling (b);
final output <= maxpooling (c);
end procedure
```

FIGURE 2.8 Proposed algorithm for fault-tolerant binarized convolution neural network.

In the above figure (Figure 2.7), three kernels have one fault in each. Considering those faulty locations, the fault-tolerant mechanism bypasses those faults and gives the fault-free fully connected layer output. Figure 2.9 shows the fault-free output after applying the fault-tolerant by bassing algorithm on the mentioned faulty conditions.

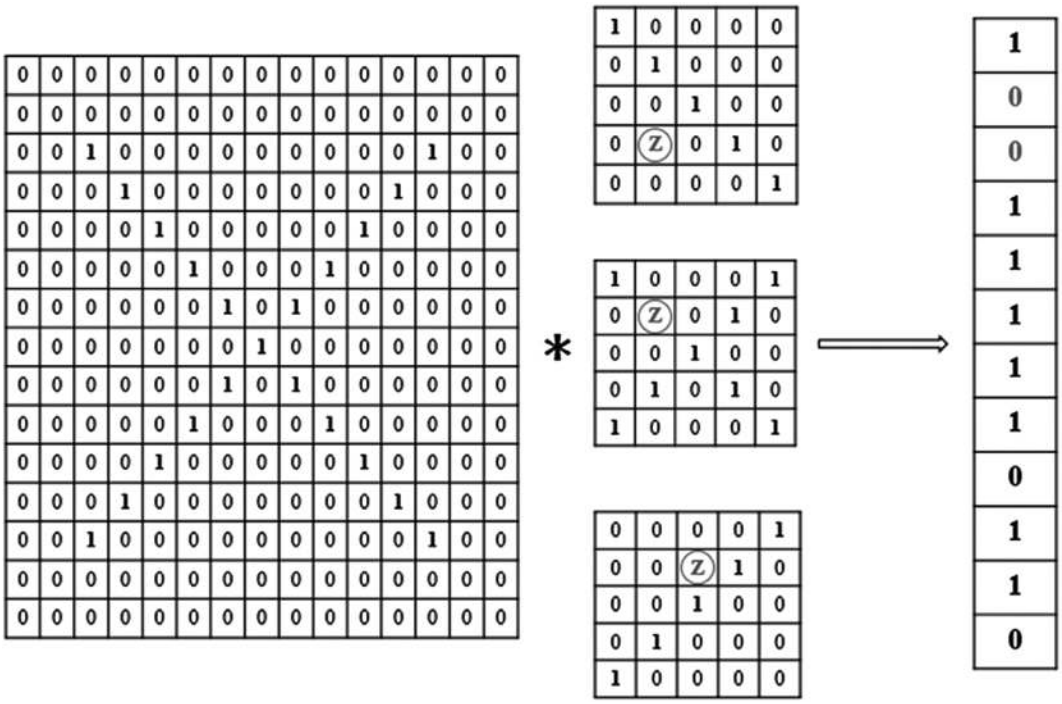

FIGURE 2.9 Fully connected output for fault-tolerant BCNN after bypassing the fault. ⏎

2.4 DESIGN IMPLEMENTATION USING XILINX FPGA

The proposed fault-tolerant algorithm has been implemented using Xilinx ISE 14.7 design tool and validated through Xilinx FPGA Artex7 (device: xc7a100t-3csg324). Figure 2.10 describes the device utilization for the implementation.

FIGURE 2.10 Device utilization summary.⏎

Device utilization summary:

Selected Device: 7a100tcsg324-3

Slice Logic Utilization:

Number of Slice Registers:	69	out	of	126800	0%
Number of Slice LUTs:	305	out	of	63400	0%
Number used as Logic:	305	out	of	63400	0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used:	354				
Number with an unused Flip Flop:	285	out	of	354	80%

Device utilization summary:					
Number with an unused LUT:	49	out	of	354	13%
Number of fully used LUT-FF pairs:	20	out	of	354	5%
Number of unique control sets:	69				
TO Utilization:					
Number of IUs:	4				
Number of bonded IOBs:	4	out	of	210	1%

The HDL synthesis report has been illustrated in Figure 2.11. The amount of adder/subtractors, latches, comparators, and multiplexers are enumerated here:

FIGURE 2.11 HDL synthesis report.

HDL Synthesis Report	
Macro Statistics	
# Adders/Subtractors	: 1815
6-bit adder	: 1815
# Latches	: 141
1-bit latch	: 141
# Comparators	: 121
6-bit comparator greater	: 121
# Multiplexers	: 289
1-bit 2-to-1 multiplexer	: 289

2.5 SIMULATION RESULTS

The experimental results for the proposed methodology have been discussed in this section. The fault-tolerant BCNN has three kinds of states. Initially, it may be considered as a normal state, without having any fault. To test the fault-tolerant algorithm, the system must be faulty. Therefore, the fault-injector has been used to inject fault into the system. A different state can be considered when a fault has been injected and that yields faulty output. Another state must be after tolerating the fault by using the

proposed fault-tolerant mechanism. Figure 2.12 illustrates the simulation result when no fault is present in the scenario.

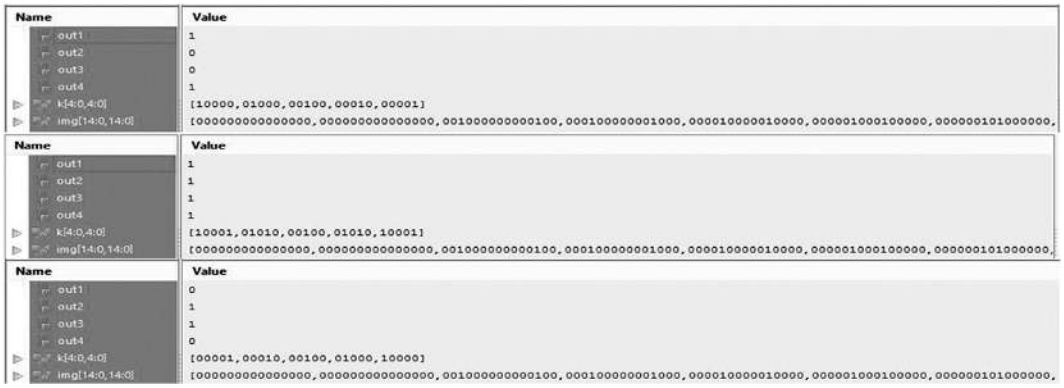

FIGURE 2.12 Simulation report: before inserting the fault (simulated in Xilinx ISE 14.7 simulator). ⏎

If the enable line of the fault-injector block is enabled, a fault has been initiated to a certain memory location of the kernel. Figure 2.13 illustrates three altered locations of different kernels, where the fault has been injected yielding faulty output. The red colored small circles represent the positions of kernels where the faults are injected and the big red circle denotes the faults reflected at the output.



FIGURE 2.13 Simulation report: after inserting the fault (simulated in Xilinx ISE 14.7 simulator). ⏎

Figure 2.14 illustrates the proposed methodology works properly and the injected faults are tolerated. Thus, the output is similar to the non-faulty condition. The smaller green circles denote the positions where faults are injected and the bigger green circle represents the output that does not have any impact on the injected fault. That means the faults are tolerated.

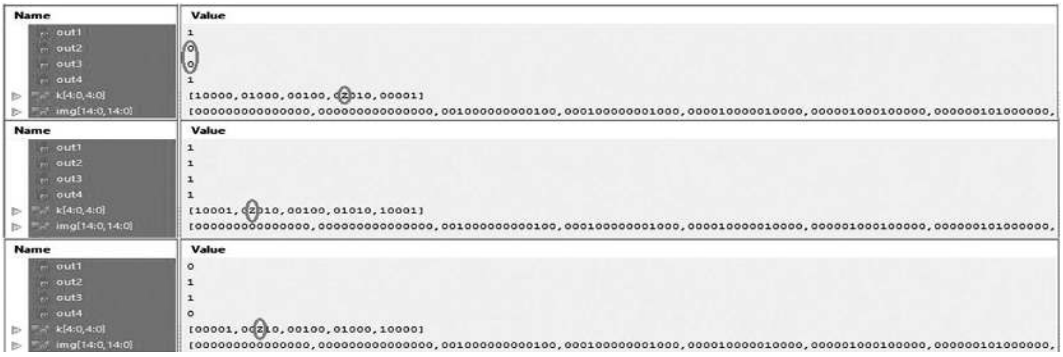

FIGURE 2.14 Simulation result: after applying the fault-tolerant algorithm (simulated in Xilinx ISE 14.7 simulator).

2.6 CONCLUSION

In this chapter, a fault-tolerant BCNN has been designed and implemented using FPGA. The CNN is a very powerful tool in the present era. Modern systems are mostly using CNN to perform several tasks such as image recognition. For safety-critical embedded systems, reliability is mostly applicable. Therefore, a single fault is not tolerable for such systems. FPGA is a robust technology to implement fault-tolerant BCNN. XILINX FPGA Artex7 (device: xc7a100t-3csg324) is used to implement the proposed methodology and simulated using the iSIM simulator. This chapter deals with SEUs and tolerates the fault by bypassing them. To handle the burst error in the kernel and to determine the fault-free output was the objective of this chapter.

KEYWORDS

- **binarized neural networks**
- **convolutional neural networks**
- **fault injection**
- **fault-tolerance**
- **FPGA**
- **kernel**
- **pooling**

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CHAPTER 3
Impact of Electromagnetic Bandgap Structure Incorporated in Square Microstrip Patch Antenna

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ABSTRACT

In the present chapter, square microstrip patch antenna design is carried out using an electromagnetic bandgap structure to achieve higher gain. Ansoft HFSS software is utilized for simulation, and optimum design parameters are set based on the predefined constraint equations and boundary conditions. Simulation output revealed higher return loss and lowering of impedance, as computed from Smith Chart, which speaks in favor of EBG structure based design. Result is suitable for implementing the structure in PhC design, at a microwave frequency spectrum.

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3.1 INTRODUCTION

Research direction toward improvement of patch antenna performance and applications due to the growing need for contemporary mobile, satellite, and wireless communication systems are investigated a lot over the last two decades [1, 2, 3, 4, 5, 6, 7, 8, 9 and 10]. In this context, both structural modifications and material-based tailoring have attained focus [11, 12, 13 and 14] owing to their unique offerings within a limited range of operating spectrum. Reconfigurable antennas have gained a lot of interest because future wireless communication systems because of their capacity to alter their geometry in response to modifications in the external environment or system specifications, including increased operating frequencies, polarizations, radiation patterns,

and bandwidths. Since microstrip antennas provide the features mentioned above, they are one of the most widely used options for creating reconfigurable antennas [15 and 16].

Owing to their desirable advantages for modern wireless communications, polarization reconfigurable antennas have gained more attention. These advantages include the ability to avoid fading loss in wireless local area networks caused by multipath effects, provide a potent modulation scheme in active read/write microwave tagging systems, realize frequency reuse to expand the capability in satellite communication systems, and be a suitable candidate in multiple-input multiple-output (MIMO) systems [17]. Wireless communication systems are now undergoing development that necessitates the use of antennas that can access services in several frequency bands, often with just one antenna. Most pattern reconfigurable antennas that have been described thus far have a restricted beam-switching range. Few antenna designs take into account both dual-frequency and radiation pattern. The overall system performance is enhanced with a multiband, pattern-reconfigurable antenna.

Owing to its suitability for high-performance aircraft, spacecraft, satellite, and missile applications—where size, weight, cost, performance, simplicity of installation, and aerodynamic profile are important limitations—low-profile antennas have garnered a lot of interest. Compact and low-profile antennas are still necessary for today's quickly evolving mobile or personal communication devices. Microstrip antennas, often called patch antennas or microstrip patch antennas, have a variety of uses [18 and 19] including satellites, commercial communication systems, and even biological applications.

Researchers have been interested in the multielement smart antenna array because of its many uses in wireless communication. Various multielement antenna prototypes are developed and put into use for base station (BS) applications in order to boost cellular capacity, coverage, and dependability as well as transmission quality. However, new developments in the research of electromagnetic band gap (EBG) structures [20, 21 and 22] have shown that these patterns may be easily solved to enhance antenna performance. An electromagnetic band gap (EBG) is a periodic structure that prevents any electromagnetic waves from propagating inside a specific frequency range. These periodic structures' stop bands are what boost performance. These configurations offer a straightforward and efficient resolution to surface and leaky wave issues. Numerous microstrip-based EBG structure types have been examined for a range of uses. Both the finite element method and the finite difference time domain are used to study these structures.

3.2 OVERVIEW OF MICROSTRIP ANTENNA

A microstrip antenna is composed of a ground plane and a conducting patch that are separated by a dielectric substrate. Many mathematical models were developed for this antenna, and its applications were extended to many other fields. Microstrip antennas are what contemporary antenna designers use. Substrates having a low dielectric constant are frequently utilized for

maximum radiation. While there are no restrictions on the shape of the conducting patch, the most common forms are round and rectangular. A microstrip antenna is defined by its length, breadth, input impedance, gain, and radiation patterns. A number of variables, related computations, and feeding methods will be thoroughly discussed in this chapter. The wavelength of the antenna's operating frequency is about half of its length. The length of the patch is important since it has an impact on the antenna's gain and return loss.

3.2.1 SURFACE WAVE EFFECT

Before the surface wave travels through the air, it reduces the amplitude of the input signal. Furthermore, spurious coupling between various circuit or antenna parts is introduced by surface waves. Because the parasitic interaction lessens the isolation in the stop bands, this impact significantly decreases the performance of microstrip filters [23 and 24]. The edges of an open microstrip construction reflect and deflect surface waves that reach their outside bounds. By increasing the side lobe and cross-polarization levels, the diffracted waves provide extra radiation that weakens the antenna pattern. Surface wave effects should ideally be reduced since they are primarily detrimental to circuits and antennas.

3.2.2 MICROSTRIP LINE

A microstrip line is a conducting layer of width "W" that is printed on a thin substrate with relative permittivity, ε_r, and thickness " h," which is a grounded dielectric. Inset feed is fed via a technology called microstrip line. Furthermore, this approach may also be used to create the electrical qualities of permeability and permittivity. Figure 3.1 displays the microstrip line diagram.

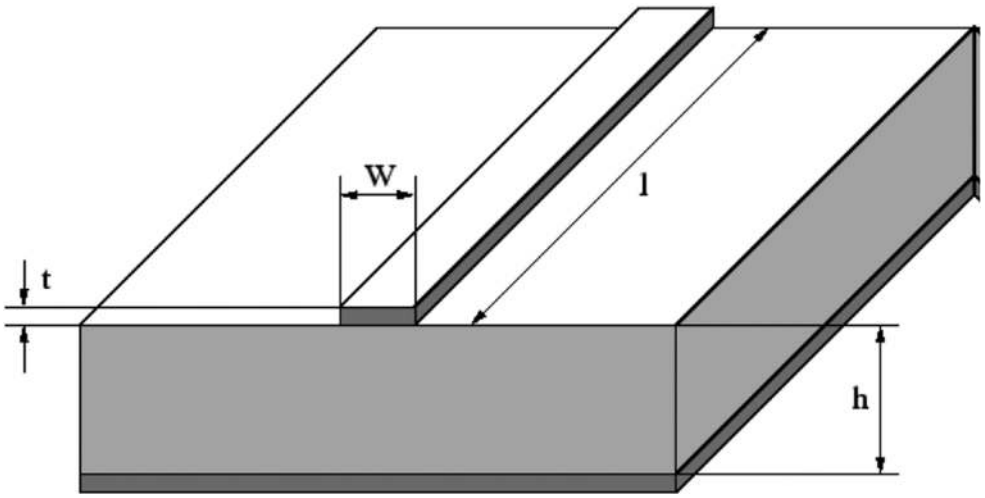

FIGURE 3.1 Microstrip line with thickness "h" and width "W."

Owing to multiple materials, dielectric constant of the structure is considered as effective, denoted by ε_{eff} as Equation 3.1:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{12h}{W}\right)^{\frac{-1}{2}} \tag{3.1}$$

Z_0, the characteristic impedance of the stripline, may be calculated as

$$Z_{0=}\begin{cases} \frac{60}{\sqrt{\varepsilon_{eff}}}\ln\left[\frac{8h}{w} + \frac{w}{4h}\right] & for\ \frac{w}{h} \leq 1 \\ \frac{120\pi}{\sqrt{\varepsilon_{eff}}}\left[\frac{w}{h} + 1.393 + 0.667\ln\left[\frac{w}{h} + 1.444\right]\right] & for\ \frac{w}{h} \geq 1 \end{cases} \tag{3.2}$$

3.2.3 RECTANGULAR PATCH ANTENNA DESIGN

The microstrip diagram and the corresponding circuit for a rectangular microstrip patch antenna are displayed in Figure 3.2. The wave's path across the ground plane and the patch is depicted by the arrows.

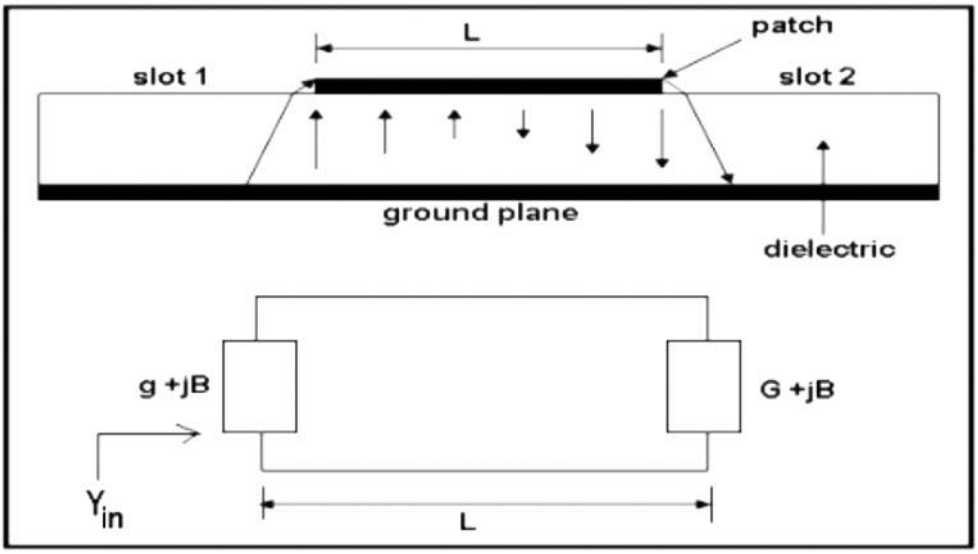

FIGURE 3.2 Microstrip diagram and equivalent circuit

The equations for traditional patch antennas were obtained from Equations 3.1 and 3.2. The following equation may be used to create traditional rectangular patch antennas, written as

$$W = \frac{c}{2f_r}\left(\frac{\varepsilon_r + 1}{2}\right)^{\frac{-1}{2}} \tag{3.3}$$

In Equations 3.3, "W" signifies width of patch antenna, "f_r" denotes frequency of operation, and "ε_r" is the substrate permittivity.

It is also important to remember that the EM fields propagate outside the microstrip patch and are not completely contained inside it. The fringing effect is the outcome of this occurrence. A capacitor is created by two parallel microstrip and ground plates; the electric field does not stop abruptly at the plate boundaries. Outside, there is a field with plates that bend in different directions. Because of this, the actual capacitance is higher than the value that was anticipated by a theoretical calculation. As a result, the effective length and effective permittivity will vary when the fringing effect is taken into account.

$$L = \frac{c}{2f_r\sqrt{\varepsilon_{eff}}} - 2\Delta l \tag{3.4}$$

where patch antenna length is designated by "L" and "c" as usual denotes speed of electromagnetic wave in vacuum.

$$\Delta l = 0.412h\left(\frac{\varepsilon_{eff}+0.3}{\varepsilon_{eff}-0.258}\right)\left(\frac{\frac{w}{h}+0.264}{\frac{w}{h}+0.8}\right) \tag{3.5}$$

The substrate length and width dimensions are calculated as Equations 3.6 and 3.7:

$$W_s = W + 6\ \mathrm{h} \tag{3.6}$$

$$L_S = L + 6\ \mathrm{h} \tag{3.7}$$

where "L_s" and "W_s" speak for substrate length and width, respectively.

3.3 FEEDING TECHNIQUES

In general, there are two types of antenna-feeding techniques: contacting and noncontacting. The microstrip line, coaxial probe (both contacting methods), aperture coupling, and proximity coupling (both noncontacting) are the four most often utilized feed mechanisms in patch antennas.

3.3.1 MICROSTRIP PATCH ANTENNA

The suggested antenna, which measures 57 × 57 × 1.6 mm^3, is driven by a microstrip feedline coupled to a 50 Ω transmission line. The square patch antenna measures 28.45 mm in width and length on the sides. The feedline measures 1.137 mm in width, 9 mm in length, and 1 mm in gap between the feed and patch. The FR4 material that makes up the substrate has a thickness of 1.6 mm, a dielectric constant of 4.7, and a 0.02 magnitude of loss tangent. To provide the patch a central feed, two slots are carved. The antenna's geometric design without an EBG is seen in Figure 3.3.

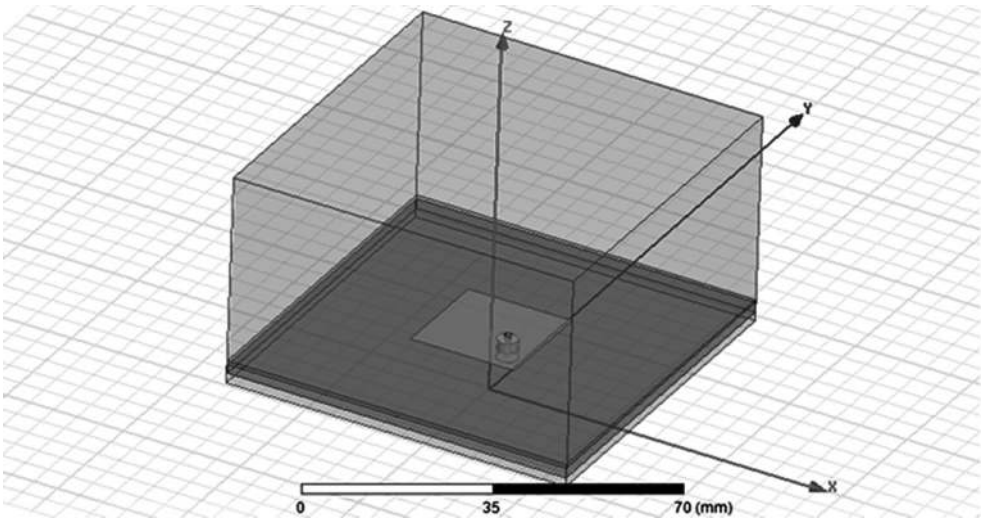

FIGURE 3.3 Microstrip patch antenna without EBG using Ansoft HFSS.

3.3.2 SQUARE MICROSTRIP PATCH ANTENNA USING SQUARE EBG STRUCTURE

Wireless applications that are low profile, conformal, and economical frequently employ microstrip patch antennas. Its poor efficiency and extremely limited impedance bandwidth, however, significantly limit its adaptability. A single-patch antenna often has relatively little gain. The gain of a patch antenna may be increased using a variety of methods. Over the substrate, a superstrate or cover layer has been employed in the resonance gain approach. To reduce the cavity underneath the patch's effective permittivity, an air gap might be inserted. The microstrip antenna's gain can be decreased by using a reduced surface-wave antenna or a parasitic element. A further option for increasing the antenna's gain is to employ an electromagnetic bandgap (EBG) construction. The microstrip antenna improves the effective radiated power and also of antenna gain significantly suppressing the surface waves induced in the substrate by the use of a square lattice of tiny metal pads and grounding vias that form a mushroom-like structure. An artificial periodic structure known as an EBG structure is the one that permits electromagnetic waves to propagate in a certain frequency range at all incidence angles and polarization states. Within the band gap region, the EBG structures suppress surface waves and stop electromagnetic waves from propagating. For optimum performance, EBG structure under consideration should satisfy the following conditions:

$$0.65 < a/p_o < 0.75 \text{ for 2D EBG}$$
$$0.9 < a/p_o < 0.95 \text{ for 3D EBG}$$

where "a" is the dimension of the mushroom patch, "p_o" indicates periodicity, "ε_r" is permittivity of the dieslectric materials used, and "a/p_o" is the filling factor.

It is determined by dividing the unit cell's periodicity by the patch sizes. Figure 3.4 displays the EBG characteristics of the mushroom type EBG. A solid patch plus a cylindrical passage make up the three-dimensional EBG structure known as the mushroom type. The dimension of the patch, via diameter, the space between the unit components, substrate material and substrate thickness are the only factors that affect the transmission properties of the mushroom-type EBG.

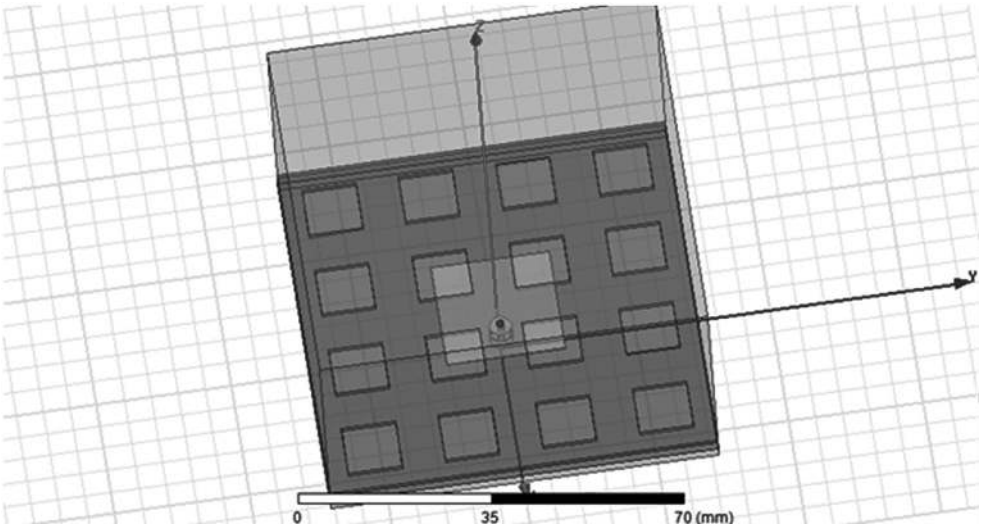

FIGURE 3.4 Microstrip patch antenna with EBG using Ansoft HFSS.

EBG structures have a larger front-to-rear ratio and a lower side lobe level. These are their primary benefits. Both single-band and dual-band EBG structures come in a variety of forms. The folk-like structure, fractaltype EBG structure, spiral-type EBG structure, hair-pin-like structure, slogan-type EBG structure, hexagonal patch-type structure, and Hilbert curve high impedance surface structure are the novel EBG structures. By employing a low dielectric substrate, increasing the substrate thickness, and using the right feeding techniques, the patch antenna's bandwidth may be increased. Surface wave losses will be smaller than the dielectric constant. In order to boost the gain of the proposed square patch antenna, a Mushroom-type EBG unit cell is utilized.

3.3.3 SQUARE MICROSTRIP PATCH ANTENNA WITHOUT AND WITH EBG STRUCTURE

The antenna is designed and simulated by using Ansoft HFSS software. The antenna performance is analyzed in terms of bandwidth, gain, and smith chart. The simulated bandwidth, gain, and characteristic impedance of the proposed antenna with EBG and without EBG structure are shown later.

Figure 3.5 shows the variation of return loss in terms of S_{11} parameter. It is seen from the figure that the central operating frequency for the given configuration is 5.04 GHz, which is very

close to the design frequency.

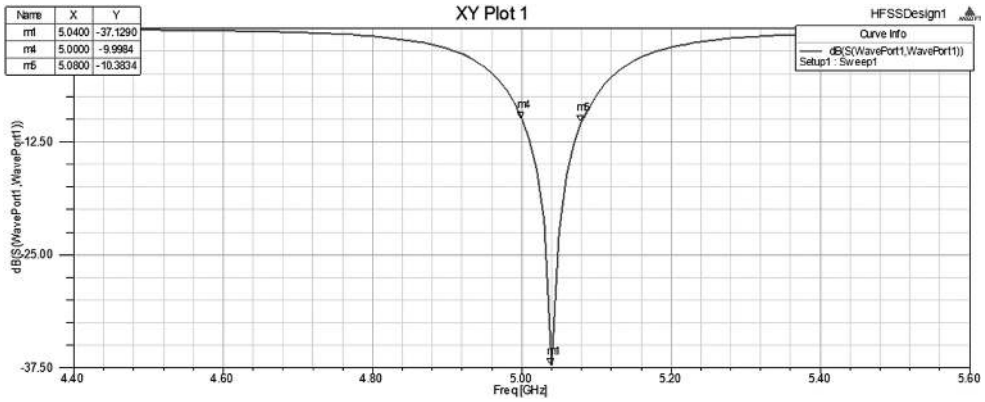

FIGURE 3.5 Return loss of microstrip patch antenna with square EBG structure.

However, when the EBG structure is not incorporated, corresponding return loss variation is represented in Figure 3.6. Also, redshift at the operating frequency is also depicted in this figure.

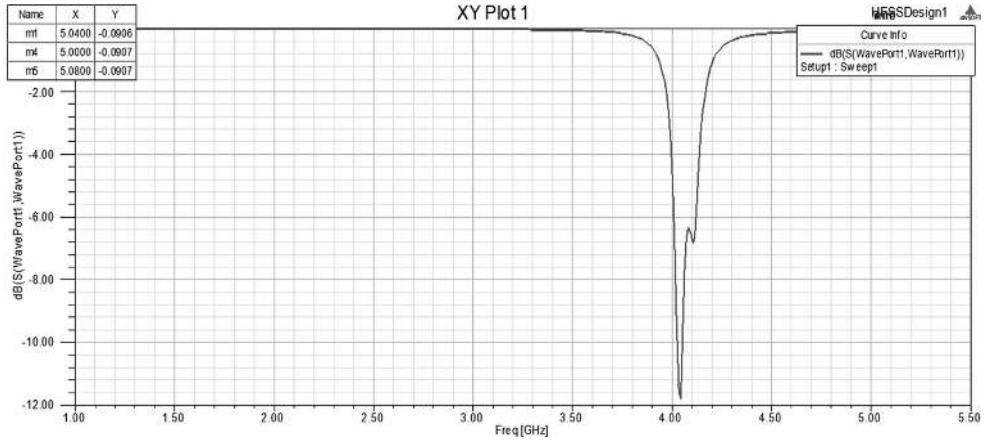

FIGURE 3.6 Return loss of microstrip patch antenna with square EBG structure.

Next gain parameter is computed for the square microstrip patch in the presence and absence of EBG structure, as reflected in Figures 3.7 and 3.8, respectively. A comparative study shows that gain increases approximately six times for the present configuration when the EBG structure is used.

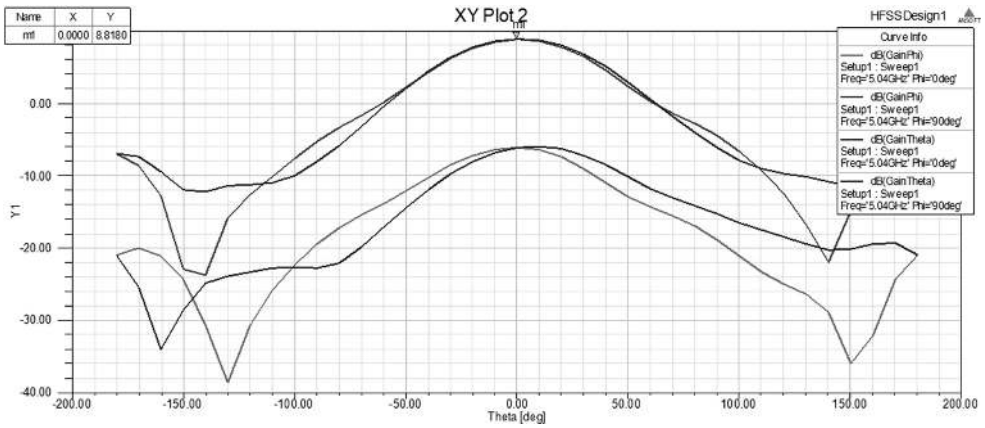

FIGURE 3.7 Gain output of microstrip patch antenna with EBG structure.

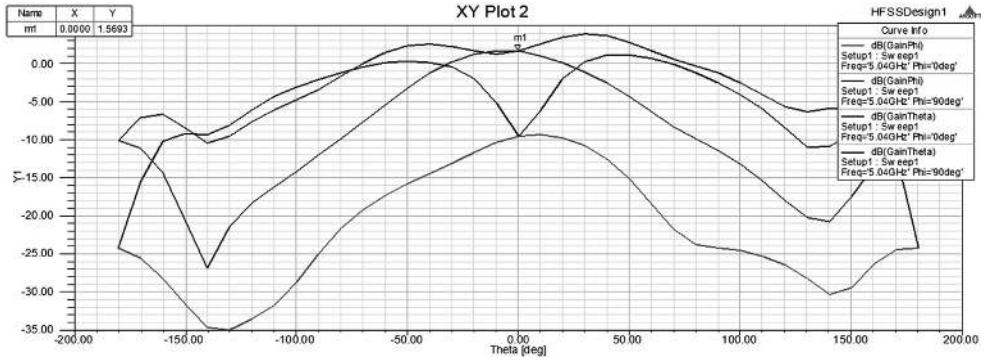

FIGURE 3.8 Gain output of microstrip patch antenna without EBG structure.

TABLE 3.1 Return Loss of the Proposed Antennas with and Without EBG.

Name	Frequency (GHz)	RL With EBG (dB)	RL Without EBG (dB)
M1	5.04	—37.1290	—0.0906
M2	5.00	—9.9984	—0.0907
M3	5.08	—10.3834	—0.0907

Figures 3.9 and 3.10 show the characteristic impedance measured using Smith chart. It is found that the resistive value of the impedance increases in the presence of EBG structure whereas reactive part decreases. The result is summarized in Table 3.3.

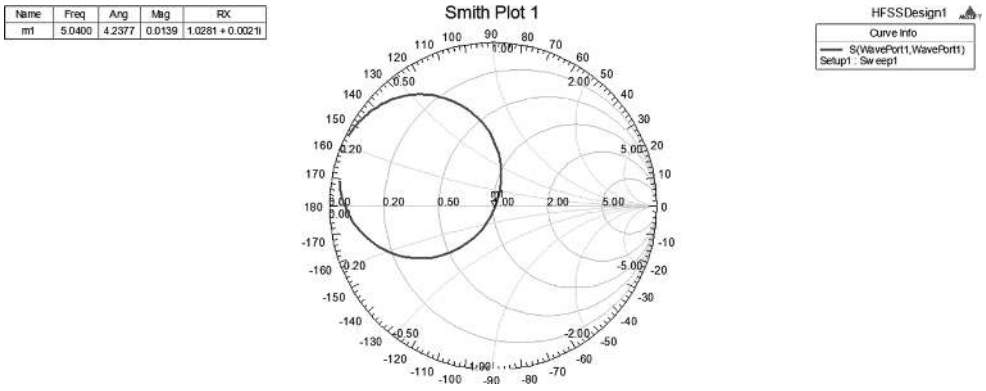

FIGURE 3.9 Characteristic impedance of microstrip patch antenna with EBG structure.

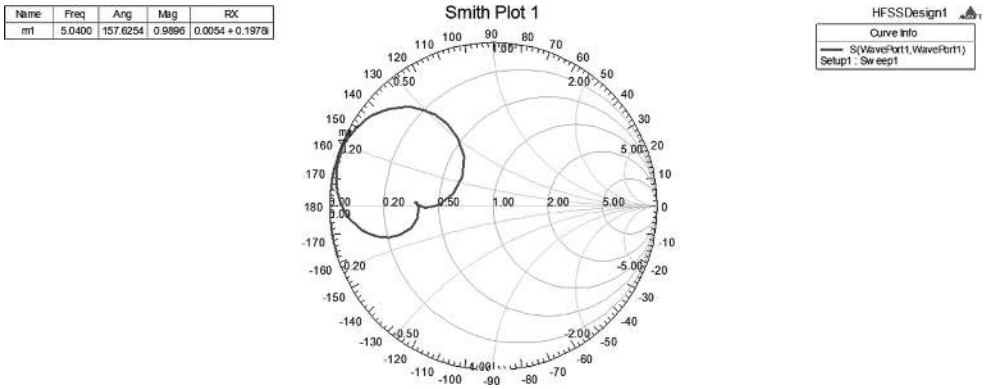

FIGURE 3.10 Characteristic impedance of microstrip patch antenna without EBG structure.

TABLE 3.3 Characteristic Impedance of the Proposed Antennas with and Without EBG.

Name	Freq.	With EBG			Without EBG		
		Avg.	Mag.	RX	Avg.	Mag.	RX
M1	5.0400	4.2377	0.0139	1.0281+0.0021 i	157.6254	0.9896	0.0054+0.1978 i

TABLE 3.2 Gain of the Proposed Antennas with and Without EBG.

Name	Angle	GAIN (dB)	
		With EBG	Without EBG
M1	0.0000	8.8180	1.56693

3.4 CONCLUSION

We use the software Ansoft HFSS 13.0 to design the antenna. The performance of the microstrip patch antenna is improved by using the electromagnetic band gap (EBG) structure, as evident from gain, return loss, and characteristic impedance profiles. In order to produce better gain, an electromagnetic bandgap structure is used in the construction **of square microstrip patch antennas. The simulation is performed using Ansoft HFSS software, and the pre-established constraint equations and boundary conditions are used to determine the ideal design parameters. According to the Smith Chart, the simulation output showed a greater return loss and a decrease in impedance, which is consistent with an EBG structure-based design. The outcome is appropriate for using the structure in the microwave frequency range for PhC design.**

KEYWORDS

- **characteristic impedance**
- **electromagnetic bandgap structure**
- **gain**
- **return loss**
- **Smith chart**
- **square microstrip patch**

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CHAPTER 4

VLSI and Random S-box Based IoT Security by Variable Irreducible Polynomial GF (2^8) in Composite Field Arithmetic

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ABSTRACT

The Internet of Things (IoT) describes a future where millions of objects and individuals are networked to transfer large volumes of data from multiple places. There are concerns about the privacy of data during the IoT's transit phases. Therefore, this chapter proposes a security method that addresses the aforementioned challenges in order to enhance trustable data exchange, specifically during distribution between an IoT and cloud-based gateway employing proposed methodology and takes less execution time compared to traditional advanced encryption standard (AES), which is suitable for IoT environment. Here the algebraic and statistical robustness of the suggested S-boxes is examined. The hardware purpose of this study is to enhance the very large scale integration (VLSI) design of the modified S-box and inverse S-box processes for the next generation of S-Boxes in composite field arithmetic. When compared to other encryption algorithms, the recommended AES design reduces the amount of time in clock-cycles required for encryption of 128 bits of information is 116 clock cycles, and the critical path delay drops from 7.49 to 6.28 ns (AES iterative design) and 6.59 ns (AES pipeline design), respectively. Therefore, the time required to finish the S-box, the AES transformation, and the AES pipeline for 128 bits of data is 2003.32, 728.48, and 764.4 ns, respectively. This is useful for IoT environment for low power comsumption. Using a hybrid suggested S-box and inverse S-box, where nine

different irreducible polynomial and key are transmitted to the cloud server, can further increase the security performance. To use a brute-force attack and decrypt the proposed random S-Box 128-bit AES key would take $1.6328450984067 \times 10^{17}$ years.

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4.1 INTRODUCTION

Internet of Things (IoT) enhances network connectivity and processing capacity for consumers, wirelessly identifiable objects, sensors, and home appliances without human intervention [1]. The IoT aims to incorporate "everything, anyone, and any service" "anywhere, anyhow, and anytime." It shows how people and organizations will use internet connection and the Internet in their daily lives to benefit from a fully connected "intelligent" future [2].

In 2015, IoT security ranked among the five most important security threats. Thus, a collective security approach is needed to establish safe and efficient IoT security solutions to harness its many benefits while using IoT for global growth. IoT security protects sensors. As more devices get connected to the Internet, hackers have more possibilities to infiltrate data. IoT devices are vulnerable to security vulnerabilities caused by data leaks. If customers don't think that their confidential information is safe, then they won't embrace IoT globally. Diverse IoT nodes can enhance attack risk if poorly linked. Unauthorized people resetting and reconfiguring IoT network devices and systems will cause security issues [3].

This chapter uses very large scale integration (VLSI) and software-based cryptography to protect IoT privacy and integrity. Smart devices [4] collect data from their environment and send it to the cloud platform. These are conscious of their physical limitations, such as limited memory, energy burning up [5, 6], cells being charged [7, 8], and computer power [9, 10, 11, 12, 13 and 14], so they cannot execute computational high complexity algorithms This chapter proposes a complex but light weight (i.e., high processing speed algorithm) encryption technique that modifies advanced encryption standard (AES) involving proposed S-box using a variable IP in GF (2^8) composite field for IoT device-cloud server data transmission.

Boolean operations and fundamental irreducible polynomials are thought to affect S-box effectiveness. The influence of primordial irreducible polynomials (IPs) was examined in Ref. [15]. To determine if IPs have an effect, consider all primitive ones. The polynomial

ring $\mathbb{Z}^2[x]$ has nine basic IPs of degree 8, hence there are nine ways to construct Galois fields GF (2^8) and nine S-boxes.

Original AES calculated the MI in GF (2^8) u the IP E(x) = $f^8+f^4+f^3+f+1$. Composite field arithmetic is used to improve all updated random S-box transition basic components in VLSI design. Additionally, combining altered and inverse S-boxes improves area efficiency. In this chapter non-linearity, Strict Avalanche, Bit Independent, linear, and differential approximation probability are utilized for algorithm security analysis and the VLSI is utilized for hardware implementation of proposed variable S-Box generation. IoT devices exclusively send IPs with a secret key, allowing recipients to generate random S-boxes. Thus, the intruder is unaware of the IP employed with every execution of the suggested AES; then out of nine IPs, any IP can be utilized. Thus, every IP introduces a modified S-box, increasing AES harder to break.

4.2 S-BOX OVERVIEW

First, the S-box procedure is explained in the following section. After that, the Galois field (2^8) and normal basis-based composite field realization of the S-box is discussed.

4.2.1 THE S-BOX

An 8-bit input is used by the S-box, which is a nonlinear operation that produces an 8-bit output. Using the IP E(x) = $f^8+f^4+f^3+f+1$, the binary field GF (2^8) can be built in the S-box. Input to the S-box will be $E = GF(2^8)$, and output will be $F = GF(2^8)$. Thus, the S-box is the affine transformation accompanied by the multiplicative inversion $E^{-1} = GF(2^8)$. Matrix (C) and vector (d) are used to produce an output using the affine transformation, which is described in 4.1.

(4.1)

$$f = Ce^{-1} + d = \begin{bmatrix} 10001111 \\ 11000111 \\ 11100011 \\ 11110001 \\ 11111000 \\ 01111100 \\ 00111110 \\ 00011111 \end{bmatrix} e^{-1} + \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \\ 0 \\ 1 \\ 1 \\ 0 \end{bmatrix}$$

4.2.2 COMPOSITE FIELD ARITHMATIC OF S-BOX

Whenever executed using a ROM, the S-box mapping used for SubBytes conversion is operationally expensive. Therefore, it is ineffective for systems that need a high throughput because ROM reading requires one full clock cycle to map one 8-bit state component, which results in sixteen clock timespan being used to change the 128 bits of information. Parallel ROMs are needed to boost throughput, which requires a huge chip surface. Therefore, employing composite field arithmetic, which implements an S-box by just using processing units, is a more practical option. The multiplication and inverse of the data in GF (2^8), along with the AT, are the first steps in the S-box substitution. The SubBytes transformation utilizing fmite field arithmetic is shown in steps in Figure 4.1.

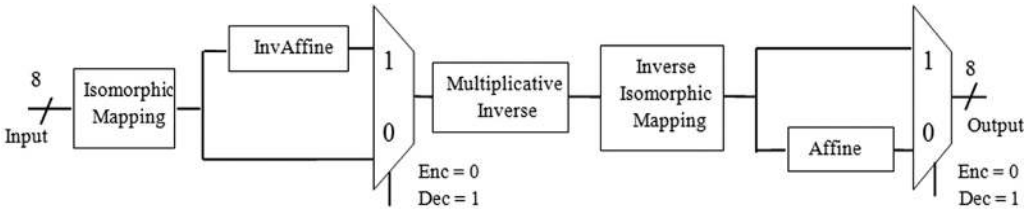

FIGURE 4.1 Substitution box conversion in finite field.

Prior to calculating the affine translation, the multiplicative inverse (MI) of GF (2^8) was first determined. Similar calculations must be made for Inv SubBytes' MI after the Inv affine transformation. Finding the MI in GF (2^8) is the only significant operation involved here. The IP x2+Fx+E can be used to represent any arbitrary polynomial in GF (2^8) as fx+e. The most important nibble in this case is (f), whereas the least important nibble is (e). Equation 4.2 can be used to determine the MI.

(4.2)

$$(fx+e)^{-1} = f\left(f^2E + feF + e^2\right)^{-1}x + (e+fF)\left(f^2F + feF + e^2\right)^{-1}$$
$$= f\left(f^2\lambda + e(f+e)\right)^{-1}x + (e+f)\left(f^2\lambda + e(f+e)\right)^{-1}$$

Where F = 1, E = λ, then produce $x^2 + x + \lambda$. Figure 4.2 displays the block diagram for using GF (2^8) to obtain the MI (2^4). The IPs and the mapping mechanism in various fields are given in Equation 4.3.

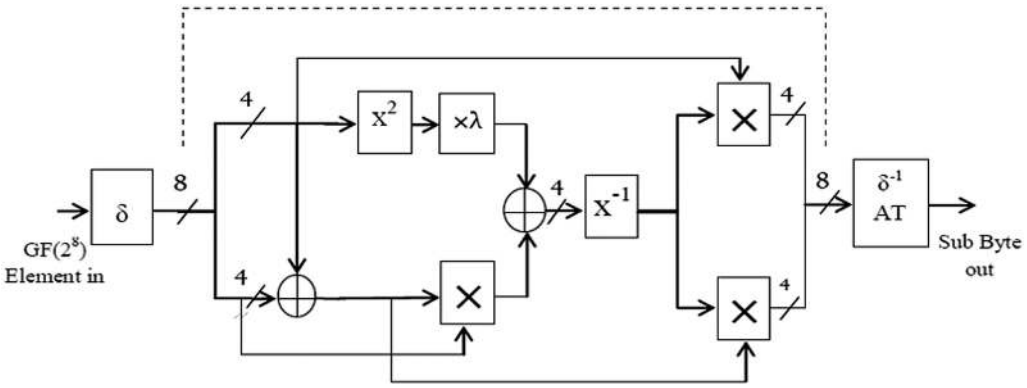

FIGURE 4.2 The conventional S-box architecture in composite field.

(4.3)

$$GF(2^2) \to GF(2) : x^2 + x + 1$$

$$GF\left((2^2)^2\right) \to GF(2^2) : x^2 + x + \phi$$

$$GF\left(\left((2^2)^2\right)^2\right) \to GF\left((2^2)^2\right) : x^2 + x + \lambda$$

In GF (2^4) × is multiplier function, X^2 is squarer, δ and δ^{-1} is the forward and inverse isomorphic mapping, AT (affine transform) is the product with constant value λ, $\oplus$ is the addition function, X^1 is the MI. The 8-bit subByte input undergoes isomorphic mapping initially. Isomorphic mapping outputs to MI unit input.

4.2.3 THE GALOIS FIELD GF(2^8)

Here are a few well-defined facts from ring and field theory. Let P be a commutative, identity-containing ring. If Q is an integral subset of P and applies to all locations and $bQ \subseteq Q$ for every $b \in P$ where $bQ = \{bq \mid q \in Q\}$, then P is a nonempty subgroup of Q and is known as a perfect of Q. Additionally, if there isn't an appropriate ideal of P that contains Q, then Q is a maximum ideal of P. Additionally, when each of P's not equal to zero portions has a necessary inverse in P, P is referred to as a field. P is an expansion of the prime field $\mathbb{Z}_l$ if l is a field of prime characteristics. If a polynomial $f(a) \in \mathbb{Z}_l[a]$ cannot be factored $\mathbb{Z}_l[a]$ into two definitely shorter polynomials, then polynomial is referred to as irreducible. The fundamental ideal, created by a monic IP $f(a) \in \mathbb{Z}_l[a]$. In the event $f(a)$ that is of degree m, the quotient ring defined is given in Equation 4.4.

(4.4)

$$\langle f(a) = \{h(a)f(a) : h(a) \in \mathbb{Z}_l[a]\rangle$$

Equation 4.5 defined the enhanced version field $\mathbb{Z}_l$ with l components and a degree of n. This field is referred to as a Galois field, indicated by the symbol GF(l^n), considered as the field expansion $\mathbb{Z}_l$ of the IP $f(a)$. A maximal optimal solution in $\mathbb{Z}_l[a]$ is a representative produced by a monic IP $f(a) \in \mathbb{Z}_l[a]$. In the event $f(a)$ that is of degree n, the quotient ring.

(4.5)

$$\frac{\mathbb{Z}_l[a]}{\langle f(a)\rangle} = \{g(a) + \langle f(a)\rangle : g(a) \in \mathbb{Z}_l[a]\},$$

Furthermore, it argues that $f(a)$ is primitive if δ is a generator of $\mathbb{Z}_l(\delta)$ defined in Equation 4.6.

(4.6)

$$\mathbb{Z}_i(\delta) = \left\{b_0 + b_1\delta + \ldots + b_{n-1}\delta^{n-1} : b_i \in \mathbb{Z}_i, \forall i\right\},$$

4.3 EXISTING WORKS

Teng et al. [16] upgrade AES S-box hardware. The study suggested that composite field arithmetic optimizes all S-box design in the SubBytes conversion. A hybrid S-box/inverse S-box design can also boost area utilization. GF $((2^2)^2)$ has a lower multiplier area. Balancing and cascaded designs increase throughput. The architecture achieves 5.79 Gbps throughput, 10% more than the prior research.

AES S-boxes, which utilize three innovative system configurations in the reverse, composite, and forward data paths, have garnered the most interest in cryptography [17]. Methodological methods and ASIC creation results reveal that these solutions each have the minimal AES S-box available for the category, which outperforms opponents in area and energy.

A switched-capacitor defense against electromagnetic side-channel attacks relies on the converter's carrier capacitance as the load signal's amplitude modulator [18]. A trustworthy analytic technique that predicts the connection between the key and the attacker's warning sign validates the recommended procedure, making it difficult for an intruder to recover confidential material. TVLA t-statistic decreases three-fold with shielded AES execution.

AES hardware improvement solutions for multi-level protected, better speed, and reduced power applications [19] are using a range of data channel key lengths and key growth. This method may approach energy proportional to the distance from the light source conventional

method, as per energy results. A correlation vulnerability assessment assault with fewer than 20,000 traces cannot show the proposed data plane's 32 bits long instead of the usual 128.

Wong et al. [20] construct three new S-boxes for the AES in the CFA over GF ((2 2) 2) 2) in this work. After running a series of algorithms and architectural improvement procedures, the optimal building design is chosen. Moreover, there are eight different isomorphic mappings that can be used to form a composite field. Therefore, the isomorphic mapping that produces the lowest implementation area expense is selected after a novel common subexpression elimination approach is used. At the chapter's conclusion, the higher computational hardware implementations of suggested CFA AES S-boxes have been discussed. The best case scenario uses a Cyclone II EP2C5T144C6 FPGA and produces a throughput of 3.49 Gbps by combining the use of standard algebraic expression, with seven stages of simultaneous piping.

Masoleh et al. [21] propose three AES S-box hardware solutions for forward, inverse, and mixed data routes. These models are the simplest AES S-boxes in their categories. To accomplish this, it employs a unique tower field style over standard bases and optimizes each unit in the three alternative designs. As per computation and ASIC synthesis findings, the CMOS STM 65 nm and Nan Gate 15 nm architectures outperform their counterparts in terms of area and power.

Ahmad et al. [22] provide a simple design process for the S-box/ Inv S-box by reducing the overall circuit area and critical path delay, shrinking the transistor area, and using cutting-edge technology to create a fully customized, performance-optimized CMOS layout. The critical route propagation delay is 3.235 ns, and the S-box/Inv S-box hardware expenses roughly 147 logic gates. The area of the circuit is about 39.44 m^2.

A lightweight S box design is proposed by Rana et al. [23] in order to achieve all the needs of simple cyphers. The suggested technique uses a combination of changes, including the MI in the GF (2^4) and affine transformations on a subset of IPs, to generate 4 × 4 S-boxes. To show how reliable the suggested technique is, several cryptanalyses are done on it.

Dey et al. [24] build 4-bit S-boxes by multiplying the MIs of all elemental polynomials (EPs) under the relevant IPs over the GF (2^4) by all feasible additive constants. All important 4-bit S-box cryptanalysis algorithms are applied to a set of 48 randomly generated S-boxes. This demonstrates that the created 4-bit S-boxes are more secure.

An approach was given by Kharjana et al. [25] to create shorter S-boxes, which is utilized in compact block cyphers. These are more compact S-boxes developed by adapting and streamlining the design method utilized by the AES S-box. In order to evaluate the suggested S-boxes, their cryptographic features and parameters were evaluated to those of the

traditional approach. The proposed S-nonlinearity box's value was also recalculated relative to an AES S-box to account for the differences between the two designs.

The approach to produce flexible key-dependent S-boxes built by Agarwal et al. [26] by simply supplementing one bit of key produced S-boxes with varying values. This technique is variable in nature, making it a secure block cypher as opposed to the fixed AES S-box, which is vulnerable to several algebraic assaults. It is feasible to create 256 unique S-boxes using this technique except for one IP, 1EF; all other polynomials in this approach performed as expected and produced the desired results.

4.4 CONTRIBUTION

1. In this chapter, nine random S-boxes were proposed for use in a variant of AES used for GF (2^8) instead of the single S-box used in conventional AES, a composite field is used.
2. In this study, employ the bijectiveAPA conversion, which is parameterfree.
3. Both hardware (VLSI) and software are used in the creation of the suggested random S-Box.
4. The weak processing ability, memory capacity, and battery capacity of IoT devices make it impossible for them to execute extremely demanding and complex encryption schemes. Through using proposed method, it takes 0.39 s to calculate 10,000 characters. In IoT, it is useful. As a result, the proposed approach offers two advantages: increased speed and increased security due to the usage of modified AES.
5. Several algebraic and statistical strengths have been examined here to analyze the efficacy of the recommended S-boxes. The bulk of logic evaluation findings support the idea that the recommended S-boxes are ideal to work with secure communication methods.
6. The proposed S-boxes were tested using brute-force crytotanalysis attacks, which would take $1.74224572 \times 10^{41}/1.067 \times 10^{24}$ years to break the algorithm and reduced the amount of clock cycles and critical path latency.

4.5 MODIFIED S-BOX BASED AES ARCHITECHTURE IN IOT FRAMEWORK

In Figure 4.3, a recommended strategy for maintaining the integrity of provided sensitive information and data via IoT gadgets is given. A modified AES method with random S-box generation is used to encrypt the discovered data in the smart devices before it is transferred to a cloud server. Once the data has been sent to the cloud, it must first be decrypted before the original discovered information can be retrieved.

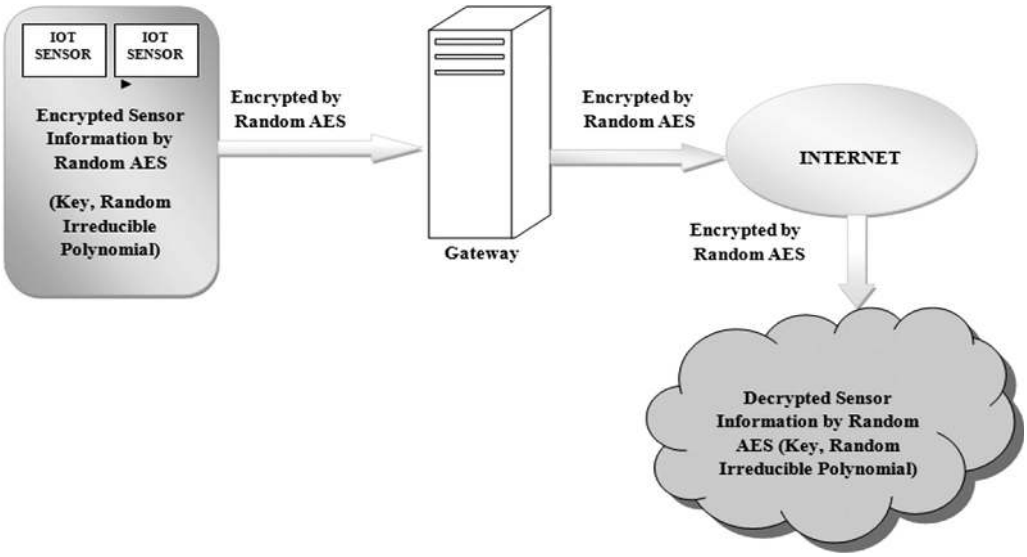

FIGURE 4.3 Suggested IoT security architecture with different sensors and VLSI platform.

In this research, an intelligent IoT system is utilized, which includes the various IoT sensors depicted in Figure 4.3. One of the most pressing problems with sending information over the Internet is that its privacy can be easily breached through eavesdropping or other forms of hostile attacks. As shown in Figure 4.3, for instance, the sensor stores sensitive information that an eavesdropper could use to prove their identity to the cloud service. Before being sent to the cloud network, smart device data is encrypted using a suggested AES with variable S-box generation by changing IP, as well as the initial observed information is retrieved from the cloud server after being decrypted.

4.5.1 HARDWARE ARCHITECHTURE AND IMPLEMENTATION

Figure 4.4 depicts the conventional structure, while Figure 4.5 depicts the proposed structure, both of which are used to explain the construction of the S-box design procedure in VLSI domain. To increase AES techniques' efficiency in space, the suggested model makes use of symbols like ß, AT, (.)-1, $(.)^{-2}$, X.

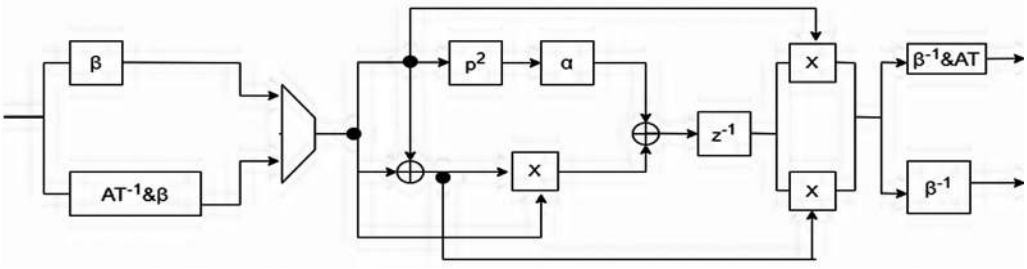

FIGURE 4.4 The standard VLSI S-box architecture.

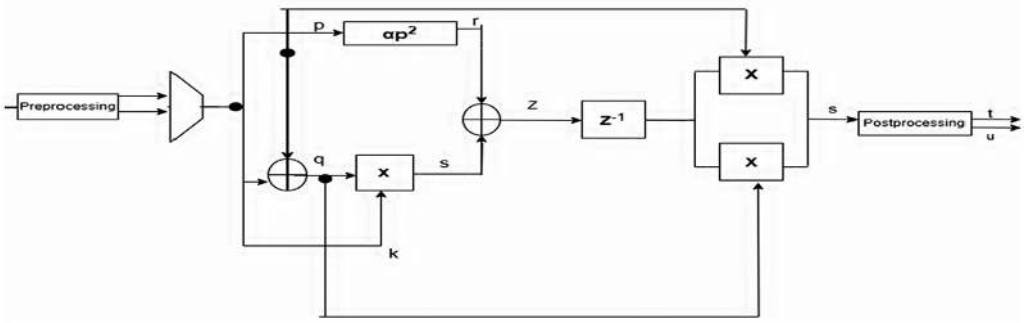

FIGURE 4.5 An S-box design on VLSI.

To construct a symmetrical framework at alternative pipeline phases without requiring a huge increase in pipelined registers, a five-stage joint S-box and inverse S-box is created, as shown in Figure 4.6. Eleven 4-bit registers are a part of the pipelined design. The second stage of the significant route in this design employs four exclusive-or (XOR) gates and one AND gate.

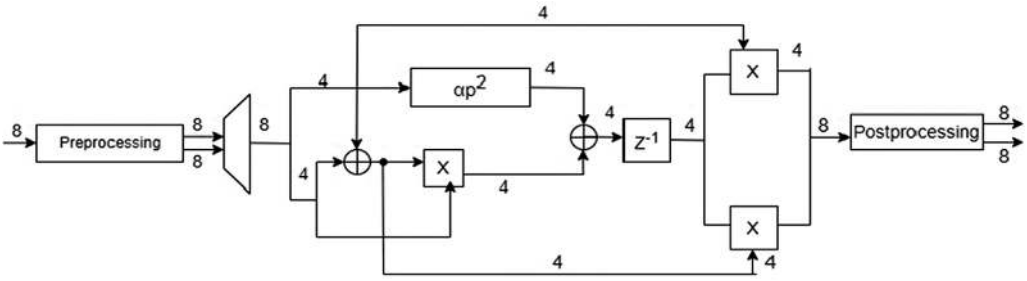

FIGURE 4.6 Integration of S-box in a pipeline with five phases.

4.5.2 VLSI IMPLEMENTATION OF AES SUBBYTES TRANSFORMATION

VLSI speed and area minimization research has been the most difficult. This study proposes S-box in VLSI architecture. The architecture is FPGA-implemented and compared to existing transformation approaches. The proposed design is low-power and delayed.

After three changes, S-box presented a new architecture.

1. Once certain blocks were merged, an operator (op) was added.
2. Employing a multiplexor to construct the MI in the GF (2^4).
3. Decreased the crucial route of multiplication GF (2^2).

4.5.2.1 ONCE CERTAIN BLOCKS WERE MERGED, AN OPERATOR (OP) WAS ADDED

Using the GF irreducible converting approach as well as the form of an input bit stream, the op equation has been presented. Getting the MI in GF (2^8) is one of the key operations here.

To accomplish this, separate the GF (2^8) elements in GF (2^4). For example, using an IP x^2+Fx+E, may be written as fx+e. The most important nibble in this case is (b), whereas the least important nibble is (c). The following phrase [27] can be used to get the MI.

(4.7)

$$(fx+e)^{-1} = f\left(f^2E + feF + e^2\right)^{-1}x + (e+fF)\left(f^2F + feF + e^2\right)^{-1}$$
$$= f\left(f^2\lambda + e(f+e)\right)^{-1}x + (e+f)\left(f^2\lambda + e(f+e)\right)^{-1}$$

where the IP in use is F = 1, E = λ

The expression f^2 λ+e (f+ e) in Equation 4.8 can be written as:

(4.8)

$$f^2\lambda + fe + e^2 = f(f\lambda + e) + e^2$$

Representing f, e, and λ as,

$$f = f_{\mathrm{H}}\mathrm{X} + f_{\mathrm{L}}, e = e_{\mathrm{H}}\mathrm{X} + e_{\mathrm{L}}, \lambda = \lambda_{\mathrm{H}}\mathrm{X} + \lambda_{\mathrm{L}}$$

In the same way that f_H and f_L, represent the highest and lowest two bits of f, e_H and e_L represent the highest and lowest two bits of e and λ_H and λ_L represent the highest and lowest two bits of λ. The fλ, is expressed as:

(4.9)

$$f\lambda = f_H\lambda_H x^2 + f_L\lambda_H x$$

And therefore,

(4.10)

$$f\lambda + e = f_H\lambda_H x^2 + f_L\lambda_H x + e_H x + e_L$$

Now from Equation 4.11,

(4.11)

$$f(f\lambda + e) = \left(f_H\lambda_H x^2 + f_H\lambda_H + e_H x + e_L\right) \times (f_H x + f_L)$$
$$= \left(f_H^2\lambda_H\varphi + f_H^2\lambda_H + e_H f_H + e_L f_H + f_L^2\lambda_H + f_L e_H\right)x + \left(f_L e_L + f_H^2\lambda_H\varphi + f_H e_H\varphi\right)$$

Here, λ = $(1100)_2$ and φ = $(10)_2$. The number is calculated using the terminology of the upper (b) band lower (c) quantum, and input bits by performing tasks in GF (2^2)2^2). By comparing the suggested design to the standard S-box architecture, it may decrease the number of blocks.

4.5.2.2 Employing A Multiplexor To Construct The Multiplicative Inverse In The Gf(24)

MI, the critical path of the model, consists of the two main components— multiplication in GF (2^4) and the sign x-1 for MI in GF (2^4). Complex logic is provided by Ref. [28] for MI in GF (2^4).

$$l_3^{-1} = l_3 + l_3 l_2 l_1 + l_3 l_0 + l_2$$
$$l_3 l_2 l_1 l_0 \tag{4.12}$$

$$l_2^{-1} = l_3 l_2 l_1 + l_3 l_2 l_0 + l_3 l_0 + l_2 + l_2 l_1$$
$$l_1^{-1} = l_3 + l_3 l_2 l_1 + l_3 l_2 l_0 + l_2 l_0 + l_2 + l_1$$
$$l_0^{-1} = l_3 l_2 l_1 + l_3 l_2 l_0 + l_3 l_1 + l_3 l_1 l_0 + l_3 l_0 + l_2 + l_2 l_1 + l_2 l_1 l_0 + l_1 + l_0$$

where, $l_3^{-1}, l_2^{-1}, l_1^{-1}, l_0^{-1}$ is the XOR operation on a 4-bit MI value $l_3 l_2 l_1 l_0$, and the plus sign denotes a 4-bit value. Several XOR gates are obviously needed for MI to be implemented in GF (2^4). The XOR gates can be removed to lessen the time delay and board area. MI in GF (2^4) input and output combinations are shown in Table 4.1. All of the possible inputs can be split in half, with no inputs being more common than any other. MSB will be set to 0 for the first half and 1 for the second. A multiplexer can achieve this by combining three input bits to produce a 4-bit output when the MSB is set to "0." (except MSB). Similarly, if the MSB is set to "1," then the input combination for the four bits outcome (MSB excluded) is going to be bits of information. Three input bits are sufficient to express the logical combination of both the opening and closing segments.

TABLE 4.1 Multiplicative Inverse in Galois Field (2^4).

I/P of Multiplicative Inverse in GF(24)	**O/P of Multiplicative Inverse in GF(24)**	
*l*3*l*1*l*1*l*0	$l_3^{-1} l_2^{-1} l_1^{-1} l_0^{-1}$	
0000	0000	First half
0001	0001	
0010	0011	
0011	0010	
0100	1111	
0101	1100	
0110	1001	
0111	1011	
1000	1010	Second half

I/P of Multiplicative Inverse in GF(24)	O/P of Multiplicative Inverse in GF(24)
1001	0110
1010	1000
1011	0111
1100	0101
1101	1110
1110	1101
1111	0100

A multiplexer allows for one of the outputs to be chosen based on the most significant bit (MSB) of the input. In Equations 4.13A and B, only OR and AND gates are present in the combinational logic, not XOR gates.

$$l_3^{-1} = \left(l_2 l_1 l_0\right) or \left(l_2 \bar{l}_1 l_0\right) or \left(l_2 l_1 l_0\right) or (l_2 l_1 l_0) \tag{4.13a}$$

$$l_2^{-1} = \left(l_2 l_1 l_0\right) oor \left(l_2 \bar{l}_1 l_0\right)$$

$$l_1^{-1} = \left(l_2 l_1 l_0\right) \text{ or } \left(l_2 l_1 l_0\right) \text{ or } \left(l_2 l_1 l_0\right) \text{ or } (l_2 l_1 l_0)$$

$$l_0^{-1} = \left(l_2 l_1 l_0\right) or \left(l_2 l_1 l_0\right) or \left(l_2 l_1 l_0\right) or \left(l_2 l_1 l_0\right) or (l_2 l_1 l_0)$$

$$l_2^{-1} = \left(l_2 l_1 l_0\right) \text{ or } \left(l_2 l_1 l_0\right) \text{ or } \left(l_2 l_1 l_0\right) \text{ or } \left(l_2 \bar{l}_1 l_0\right) \text{ or } \left(l_2 l_1 l_0\right) \text{ or } (l_2 l_1 l_0) \tag{4.13b}$$

$$l_1^{-1} = \left(l_2 l_1 l_0\right) \text{ or } \left(l_2 l_1 l_0\right) \text{ or } \left(l_2 l_1 l_0\right) \text{ or } \left(l_2 \bar{l}_1 l_0\right)$$

$$l_0^{-1} = \left(l_2 l_1 l_0\right) \text{ or } \left(l_2 l_1 l_0\right) \text{ or } \left(l_2 l_1 l_0\right)$$

4.5.2.3 Decreased The Crucial Route Of Multiplication Gf (22)

The 4:1 multiplexer, down from two in the typical design is used. Multi-plication in GF (2^2) uses 2-bit inputs (x, y) and produces a 2-bit output (z) shown in Figure 4.7.

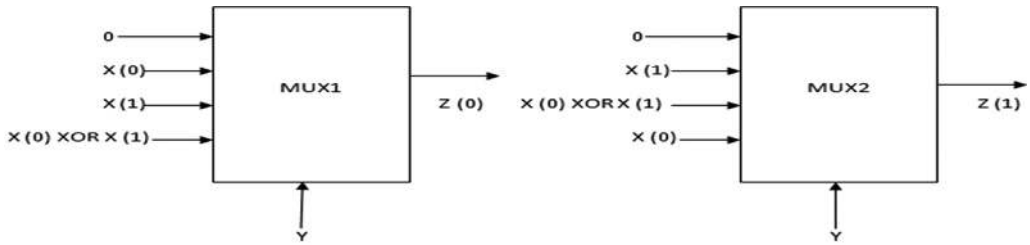

FIGURE 4.7 Two bits of multiplier output from a 4:1 multiplexer in GF (2^2).

The building procedure for each of the nine different S-boxes is shown in flowchart form in Figure 4.8. Additionally, Figure 4.8 depicts the creation of S-boxes corresponding to

polynomials 1 (E_1) through 9 (E_9). Figure 4.8 shows all of the S-boxes, which correspond to E_1 through E_9.

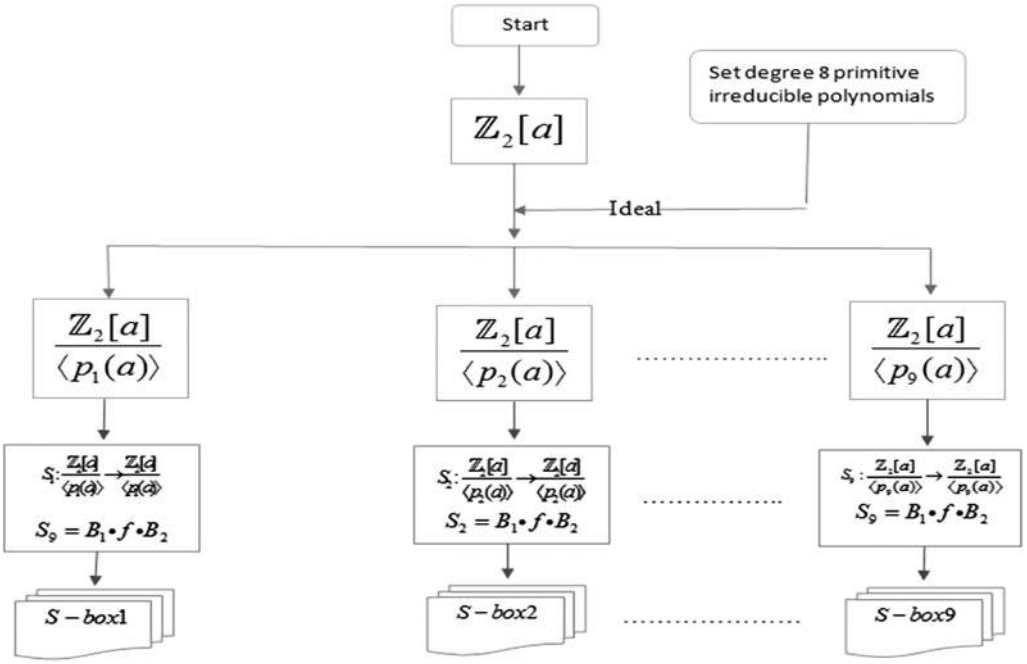

FIGURE 4.8 Flow chart for generating the suggested S-boxes for corresponding IP E_1 and E_9.

4.5.3 SOFTWARE ALGORITHM

The method to estimate MI is shown in Equation 4.14.

(4.14)

$$l_i' = l_i \oplus l_{(i+4) \bmod 8} \oplus l_{(i+5) \bmod 8} \oplus l_{(i+6) \bmod 8} \oplus l_{(i+7) \bmod 8} \oplus c_i$$

Since the prime (′) in Equation 4.15 shows that the quantity on the correct side should be used to alter the variable, that is what should be done. The AES's matrix below depicts this transition.

(4.15)

$$\begin{bmatrix} l'_0 \\ l'_1 \\ l'_2 \\ l'_3 \\ l'_4 \\ l'_5 \\ l'_6 \\ l'_7 \end{bmatrix} = \begin{bmatrix} 10001111 \\ 11000111 \\ 11100011 \\ 11110001 \\ 11111000 \\ 01111100 \\ 00111110 \\ 00011111 \end{bmatrix} \begin{bmatrix} l_0 \\ l_1 \\ l_2 \\ l_3 \\ l_4 \\ l_5 \\ l_6 \\ l_7 \end{bmatrix} \oplus \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \\ 0 \\ 1 \\ 1 \\ 0 \end{bmatrix}$$

Initialize

Remd[1] = L_1[1], Remd[2]=L_2[2], Auxl[1] = C_l[1], Auxl [2]= C_2[1], Quotn[p] = Q[p]

$$L_1[1] := z(x)$$
$$L_2[2] := y(x)$$
$$C_1[1] := 0$$
$$C_2[2] := 1$$
$$t := 2$$

while L [t] > 1

$$t := t + 1$$
$$L[t] := Remd(L[t-2]/L[t-1])$$
$$Q[t] := Quotn(R[t-2]/R[t-1])$$
$$C[t] := Q[t]*C[t-1] + C[t-2]$$

Multiplicative inverse: = C[t]

Analysis techniques such as nonlinearity, SAC, BIC, LP, and DP verify the robust cryptographic features of these random S-boxes.

4.6 EXPERIMENTAL RESULTS

The research was performed on a Windows 10 loaded with an Intel (R) Core (TM) i3-4170 CPU at 3.70 GHz and 8 GB of RAM using the Python IDE 3.11.1 interpreter. All results were visualized with the help of Python's plotting module (Matplotlib). Xilinx's design suite 14.5 is used to create the VLSI.

The proposed variable S-box and the inverse S-box generation method are used to create nine different S-boxes, and the resulting inverse S-boxes are verified experimentally. The nine IPs mentioned below provide the necessary S-box and inverse S-box for the finite field GF (2^8). In contrast to the single S-box and single IP produced by conventional AES in the

GF (2^8) finite field, the nine S-boxes and nine IPs produced by the new approach are a significant improvement. Figure 4.9 shows a time comparison between regular AES and the proposed method.



FIGURE 4.9 Comparative analysis of execution time.

4.6.1 NINE IRREDUCIBLE POLYNOMIAL

Out of a total of 43 IPs, only nine yield precise inverse S-box findings in the fmite field GF (2^8). MI is shown in Figure 4.10, and the right S-box and inverse S-box IP are shown in Figure 4.11. The red circles identify the correct MI, S-box, and inverse S-box.

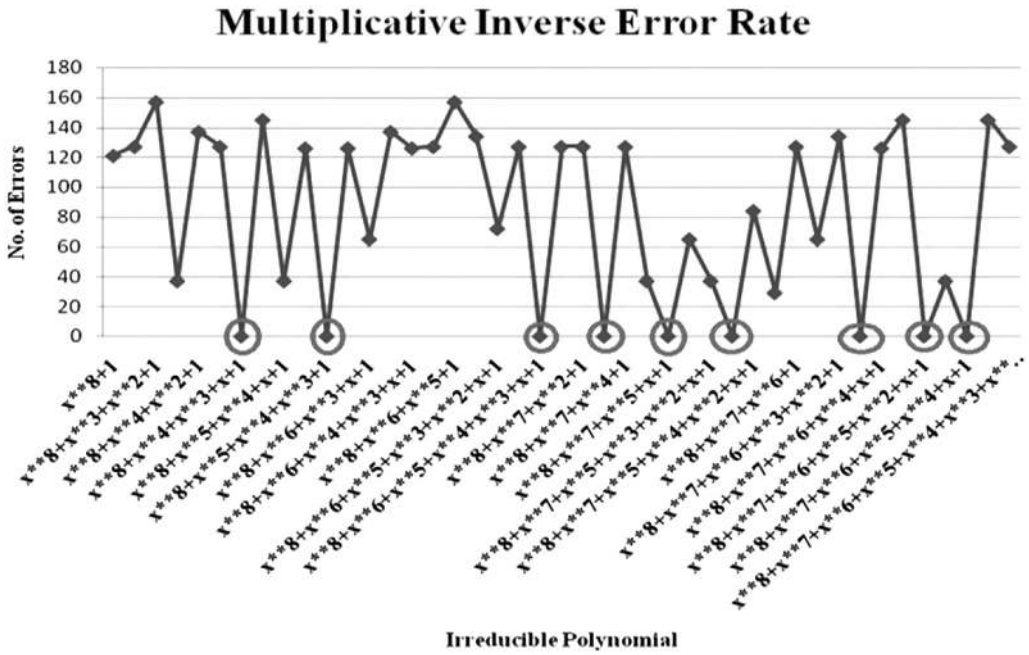

FIGURE 4.10 Multiplicative inverse corrected irreducible polynomial.

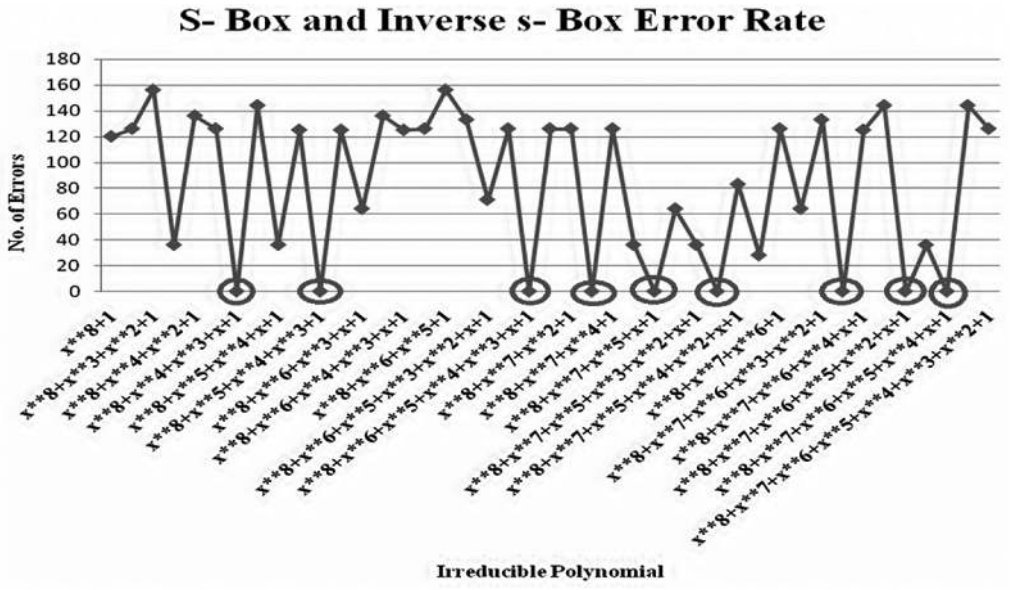

FIGURE 4.11 S-box and inverse S-box corrected IP.

$$E_1(x)=f^8+f^4+f^3+f+1$$
$$E_2(x)=f^8+f^5+f^4+f^3+1$$
$$E_3(x)=f^8+f^6+f^5+f^4+f^3+f+1$$
$$E_4(x)=f^8+f^7+ f^3+f^2+1$$
$$E_5(x)=f^8+f^7+f^5+f+1$$
$$E_6(x)=f^8+f^7+f^5+f^4+1$$
$$E_7(x)=f^8+f^7+f^6+f^3+f^2+f+1$$
$$E_8(x)=f^8+f^6+f^5+f^4+f^3+f+1$$
$$E_9(x)=f^8+f^7+f^6+f^5+f^4+f+1$$

Total nine correct S-box, inverse S-box, and MI are shown in Figure 4.11.

4.6.2 SECURITY ANALYSIS

Some algebraic and statistical analyses of the S-box are presented in this section.

4.6.2.1 Nonlinearity

Analyzing a function's nonlinearity *f* requires finding the smallest hamming gap that exists Boolean function *f*: *f*: $\{0,1\}^m \rightarrow \{0,1\}$. The nonlinearity *f* of the Boolean truth table f_1 is a measure of how different *f* is from every affme function. An indicator of a function's nonlinearity is how large its minimum hamming distance is. Large nonlinearity is known to protect against assaults using linear approximations [22, 23]. The calculation of upper limit of nonlinearity is $M = 2^{m-1} - 2^{(m/2)-1}$. As a result of these calculations $m = 8$, here the

maximum value of nonlinearity can be 130, which is the value that works best. To illustrate the nonlinearity of all basic IPs, Table 4.2 displays the nine S-boxes and this is clear from this table that the presence of an IP in the background does not reduce the value of nonlinearity.

TABLE 4.2 Nonlinearity of the Suggested S-Box.

S-boxes	**f_1**	**f_1**	**f_1**	**f_1**	**f_1**	**f_1**	**f_1**	**f_1**	**Avg**
S-box 1	130	130	130	130	130	130	130	130	130
S-box 2	130	130	130	130	130	130	130	130	130
S-box 3	130	130	130	130	130	130	130	130	130
S-box 4	130	130	130	130	130	130	130	130	130
S-box 5	130	130	130	130	130	130	130	130	130
S-box 6	130	130	130	130	130	130	130	130	130
S-box 7	130	130	130	130	130	130	130	130	130
S-box 8	130	130	130	130	130	130	130	130	130
S-box 9	130	130	130	130	130	130	130	130	130

4.6.2.2 Sac

Using the ideas of totality and wholeness, the strict avalanche criteria (SAC) as described in Ref. [29]. The probability that when one i/p bit is altered to a near value of 50%, the o/p bits will likewise get altered. It aids in demonstrating that it is impossible to determine the shape of the output vector from modifications in the input vector, and that the output vector is highly random [30]. By all measures of S-box effectiveness, the modified S-boxes meet that standard with the security and acceptance criteria. All nine of the suggested S-boxes and their corresponding SAC values are shown in Table 4.3. This data demonstrates that the highest possible SAC for the nine S-boxes is 0.57167. Similarly, the nine S-boxes have a minimum SAC value of 0.42833. The range [0.49371-0.51847] is where the expected average of SAC is located.

TABLE 4.3 Strict Avalanche Criteria.

S-Boxes	**Max**	**Min**	**Avg**
S-box 1	0.57167	0.42833	0.49526
S-box 2	0.55128	0.44872	0.49371
S-box 3	0.57167	0.47510	0.51631
S-box 4	0.57167	0.44872	0.5028
S-box 5	0.55128	0.47510	0.51847
S-box 6	0.57167	0.42833	0.49013
S-box 7	0.57167	0.42833	0.50168

S-Boxes	Max	Min	Avg
S-box 8	0.57167	0.47510	0.51731
S-box 9	0.57167	0.44872	0.50385

4.6.2.3 Bit Independent Criterion

Detombe and Tavares provide another bit independent criterion (BIC) for assessing the efficacy of S-boxes as described in Ref. [31]. The results are shown in Table 4.4. The first S-box has the lowest BIC to SAC ratio, at 0.46381, and the sixth S-box has the highest, at 0.49573. Between 0.4926 and 0.50628 is where most calculations for BIC to SAC land. As a whole, all S-boxes have a BIC no lower than 114 and no higher than 114. These modified S-boxes are shown to provide the best approximation of BIC evaluations.

TABLE 4.4 Bit Independent Criterion.

S-box	BIC-SAC		BIC	
	Minimum	Average	Maximum	Average
S-box 1	0.46381	0.50183	114	114
S-box 2	0.47921	0.49261	114	114
S-box 3	0.46726	0.50378	114	114
S-box 4	0.47629	0.50481	114	114
S-box 5	0.48531	0.50628	114	114
S-box 6	0.49573	0.49583	114	114
S-box 7	0.46329	0.50371	114	114
S-box 8	0.48385	0.50385	114	114
S-box 9	0.47831	0.49736	114	114

4.6.2.4 Linear Approximation Probability

Matsui uses the probability of a linear estimate to define the maximum value of an imbalanced occurrence. It's important to note that the mask's input G_a and output masks G_j have the same parity. For any given S-box, the following equation describes its linear estimation probability:

(4.16)

$$LP = \max_{G_a G_j \neq 0} \left| \frac{\#\{a \in A \mid a \cdot G_a = S(a) \cdot G_j\}}{2^r} - \frac{1}{2} \right|,$$

Where G_a and G_j are the sets of input masks and corresponding output masks; the set "A" signifies the collection of all potential inputs; 2^r the number ofmembers of is. S-box resilience to linear attacks is represented by the quantity of linear approximation. The

maximum number of suggested S-boxes is 156, and their combined LP value is 0.7452 (Table 4.5). The modified S-boxes are suitable for linear attacks with these LP values.

TABLE 4.5 Probability Estimation Using Linear and Differential Approximations.

S-box	LP Maximum Number	LP	DP Maximum Amount	DP
S-box 1	156	0.7452	8	0.17485
S-box 2	156	0.7452	8	0.17485
S-box 3	156	0.7452	8	0.17485
S-box 4	156	0.7452	8	0.17485
S-box 5	155	0.7267	8	0.17485
S-box 6	155	0.7267	8	0.17485
S-box 7	156	0.7452	8	0.17485
S-box 8	156	0.7452	8	0.17485
S-box 9	156	0.7452	8	0.17485

4.6.2.5 Probability of Differential Computation (DP)

The DP of an S-box measures its amount of differential regularity. It can be written out mathematically as:

(4.17)

$$(\Delta p \rightarrow \Delta q) = \left[\frac{\#\{p \in A \mid T(p) \pm T(p \pm \Delta p) = \Delta q\}}{2^n} \right]$$

A differential i/p Δp_i, needs to be assigned to an o/p differential Δq_i individually for each i to see how many possible input values are represented by 2^n. Here the expression is used A, which gives maximum value eight and DP value 0.17485 for all nine S-boxes as shown in Table 4.5. A comparative analysis of values for the modified S-boxes and the AES S-box can be observed in Table 4.6.

TABLE 4.6 Comparative Performance Analysis of AES S-box and Suggested S-boxes.

S-box	Non-linearity	SAC	BIC	BIC-SAC	DP	LP
AES S-box	130	0.49526	114	0.50183	0.7452	0.17485
S-box 1	130	0.49526	114	0.50183	0.7452	0.17485
S-box 2	130	0.49371	114	0.49261	0.7452	0.17485
S-box 3	130	0.51631	114	0.50378	0.7452	0.17485
S-box 4	130	0.5028	114	0.50481	0.7452	0.17485
S-box 5	130	0.51847	114	0.50628	0.7267	0.17485
S-box 6	130	0.49013	114	0.49583	0.7267	0.17485
S-box 7	130	0.50168	114	0.50371	0.7452	0.17485
S-box 8	130	0.51731	114	0.50385	0.7452	0.17485
S-box 9	130	0.50385	114	0.49736	0.7452	0.17485

4.6.3 COMPARATIVE ANALYSIS OVER TRADITIONAL S-BOX AND RANDOM S-BOX

In this chapter, a visual comparison of the nine different dynamic S-boxes that can be created from a single change to an IP and the components of the AES S-box is provided. By integrating a new and variable S-box into every round of AES, the dynamic S-box method improves the security of the cypher against algebraic attacks. There have been a large number of attempted algebraic attacks on AES. Algebraic attacks examine the mathematical underpinnings of block cyphers in an effort to decipher them by comparing plaintext and ciphertext.

Attacks are launched by attackers or cryptanalysts who analyze the linear and differential properties of the AES S-box. Intuitively, all assaults are made much more complicated by the new technique given. Figure 4.12 shows the difference of element in S-box with respect to AES and Variable AES whereas Figure 4.13 and 4.14 give the percentage of difference between variable S-box.

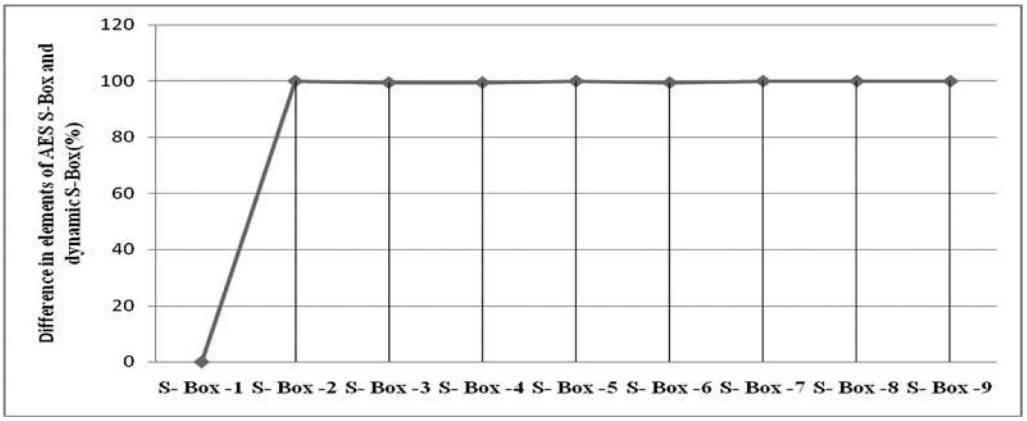

FIGURE 4.12 Comparing the static S-box and variable S-box of the elements of AES.

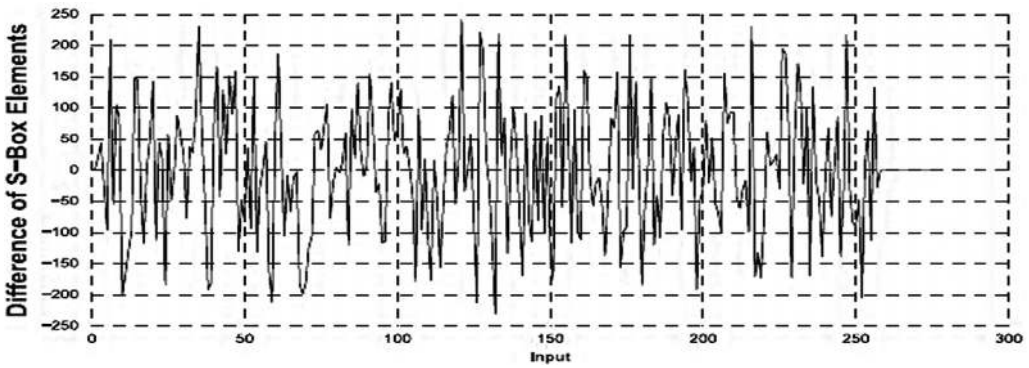

FIGURE 4.13 Display a 100% mismatch between the AES S-box and variable S-box component by IP.

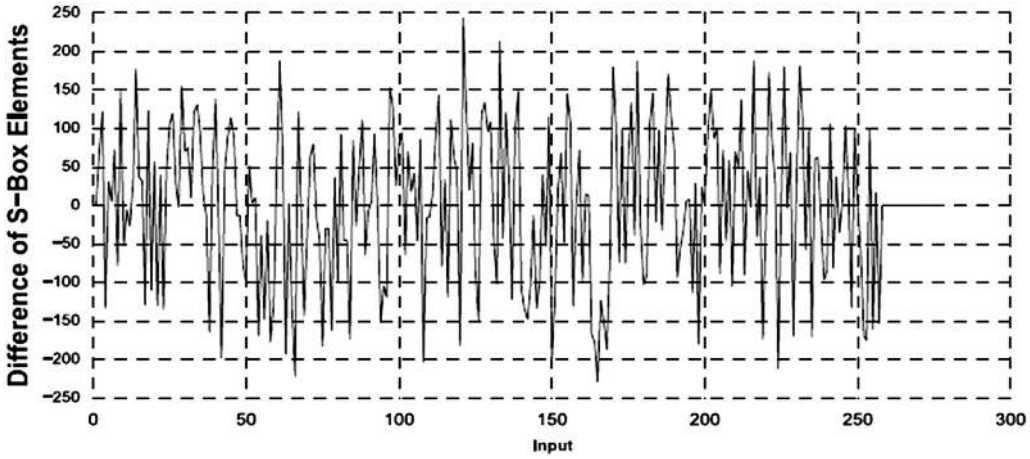

FIGURE 4.14 Display a 99.5% mismatch between the AES S-box and variable S-box component by IP.

4.6.4 COMPLEXITY ANALYSIS

4.6.4.1 Time Complexity

The AES-128-bit encryption process involves 10 iterations of all four components, with the final iteration including only three aspects (without the AddRoundKey step). The methods substitute byte, shift rows transformation, mixcolumns, and AddRoundKey Transformation all display O (1) computations on their own. Using a rough sum across all 10 rounds, here in this chapter, we find that the time complexity is O(1).

Given that P/128 = n: n ∈ N, the total time complexity of the AES-128 encryption procedure is O(n) if the plaintext size is p.

4.6.4.2 Brute Force Cryptanalysis

If we assume an AES key length of 128 bits, then we can only verify up to 2^{128} possible combinations with a brute force assault. However, the S-box is not fixed in this work; rather, it varies throughout the nine different cases presented. As a result, 2^{128}X 2^{9}= 2^{137}= $1.74224572 \times 10^{41}$, the maximum check needed for a brute force assault. The time required to launch a bruteforce attack has been quantified, all thanks to the processing power of the most recent supercomputer.

> Faster super computer: 33.86 PFLOP/s = 33.86×10^{15} FLOP/s.
> 33.86 quadrillion keys per second. [1 Quadrillion = 1,000,000,000,000,000; one thousand million million; 10^{15}; prefix peta-].
> 1 year = $365 \times 24 \times 60 \times 60$ = 31,536,000 s.
> So, $31,536,000 \times 33.86 \times 10^{15} = 1.067 \times 10^{24}$ keys per year.

As such, it's time for a brute-force attempt to decipher the new variable S-box AES-128-bit key used is = $1.74224572 \times 10^{41}/1.067 \times 10^{24}$ years = $1.6328450984067 \times 10^{17}$ years.

4.6.5 HARDWARE (VLSI) S-BOX IMPLEMENTATION

Implementations in VHDL have been made both for the traditional S-box and for the suggested S-box architectures. Different Xilinx hardware was used for the design's synthesis process. Table 4.7 compares the proposed designs to the standard designs in terms of the devices they use. Comparing the proposed solution to the standard architectures of the S-box and AES encryption algorithm reveals significant area improvement (regarding FPGA slices) and increase in performance (the key path delay).

TABLE 4.7 Comparative Analysis of VLSI S-box Implementation.

FPGA Made by Xilinx	**Spartan6 (xc6slxl6-3csg324)**				**Virtex-II pro (xc2vp30)**
Layout	**Substitution-box**		**Sequential AES**		**AES pipeline**
	Conventional logic	**with proposed logic (average of nine S-box)**	**with conventional logic (% usage)**	**Using suggested logic (% utilization)**	**Using proposed logic (% utilization)**
No. of slices	35	22	1035 (52%)	710 (35%)	8538 (64%)
No. of LUTs	94	48	3068 (36%)	1384(16.23%)	16732 (51%)
No. of slice registers	1	0	927 (7%)	682(5.14%)	4284 (16%)
Delay	19.34 ns	17.27 ns	7.49 ns	6.28 ns	6.59 ns
Power	25 mW	25 mW	27 mW	27 mW	11.47 mW

It requires additional hardware to execute the pipeline approach. Hence, pipeline architecture cannot be utilized in Spartan hardware. Spartan6 FPGA's iterative AES design requires two cycles every SubBytes transformation and eight cycles per AddRoundKeys, mixcolumns, and shiftrows transformation.

This signifies that it requires 116 clock cycles, or 10 rounds multi-plied by (8+2)+16. The new S-box design has a maximum delay of 17.27 ns, while the AES iterative design has a delay of 6.28 ns, and the AES pipeline design has a delay of 6.59 ns. To decode 128-bit data using S-box, AES transformation, and AES pipeline will take (116 × 17.27 = 2003.32), (116 × 6.28 = 728.48), and (116 × 6.59 = 764.44) ns, respectively.

4.7 CONCLUSION

Due to the massive advancements in wireless technology, the IoT is now generally acknowledged and utilized in the area of global growth. If the threats and problems associated with IoT security can be properly controlled and treated cautiously, in specific the innate facet of privacy protection when personal data is transmitted. In this research, the problems of data security during the various stages of data communication between IoT devices are addressed by employing a privacy framework enabled by cryptography. AES with random S-box—the information is transmitted between a smart device and a cloud platform using a composite field approach, which is constructed by various (9) IPs in GF

(2^8). Composite field arithmetic is used to optimize the individual components that make up the random S-box used in the transformation, hence achieving the desired result. The S-box VLSI architecture for the AES algorithm is proposed here. To encrypt 128 bits of data, the suggested AES approach minimizes the number of clock cycles to 116, and the critical path latency from 7.49 to 6.28 ns (AES iterative design) and 6.59 ns (AES pipeline design). This means that for 128-bit data, the times needed to complete the S-box, the AES transformation, and the AES pipeline are 2003.32, 728.48, and 764.4 ns. Thus, the intruder is unaware of the IP employed with every execution of the suggested AES then out of nine IPs any IP can utilized. Thus, every IP introduces a modified S-box, increasing AES harder to break. To use a brute-force attack and decrypt the proposed random S-box 128-bit AES key would take $1.74224572 \times 10^{41}/1.067 \times 10^{24}$ years.

4.8 FUTURE SCOPE

The suggested scheme has to be implemented in future works as a lightweight post-quantum cryptography for IoT devices. The field of lightweight post quantum cryptography focuses on developing new forms of cryptography that are secure against attack from both quantum and classical computers. Privacy in cryptosystems is produced by solving a specific challenge, hence these technologies can be broken down into different families. It is thought that neither classical nor quantum computers can solve these underlying problems. Because of the proliferation of IoT gadgets, efficient but lightweight cryptography has become essential. Some of the information exchanged between IoT devices is confidential, thus it is always encrypted. Thus, research into lightweight post-quantum cryptography is crucial for quantum-safe and low-overhead cryptography. So in near future the random S-box generation in finite field GF (2^8) for AES can be implemented by lightweight post quantum cryptography.

KEYWORDS

- **affine transformation**
- **avalanche bit-independent criterion**
- **composite field GF**
- **dynamic S-box**
- **IoT**
- **IP**
- **isomorphic mapping**

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CHAPTER 5

Recent Advances in Slotted Waveguide Antenna Design for its Use in Modern Microwave Remote Sensing

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ABSTRACT

Microwave remote sensing has gained significant prominence in modern scientific and technological arenas. This chapter delves into the comprehensive exploration of use of slotted waveguide arrays as a pivotal component in microwave remote sensing systems. The investigation revolves around a very detailed comparative analysis between two distinct remote sensors. One is the dual-frequency synthetic aperture radar (DF-SAR) antenna—science payload onboard the Ch-II satellite and is regarded as a cutting-edge remote sensor with outstanding performance. The other is a dual-frequency slotted waveguide array antenna (DF-SWA) with dual

polarization capability proposed by the authors and optimized to operate at the same frequencies of the DF-SAR antenna (S-Band at 2.5 GHz and L-Band at 1.25 GHz), thereby facilitating a meticulous systematic analysis and performance assessment. The first stage of the study adapts a conventional slotted waveguide design for both frequency bands. The findings demonstrate the promising potential of slotted waveguide arrays in the realm of remote sensing. However, it becomes evident that the traditional design necessitates specific modifications to enhance its attributes. In the second stage, the research implements enhancements to the conventional designs, such as incorporation of ridged waveguides for aperture blockage reduction, implementation of tapered aperture distribution for side lobe reduction, introduction of sub-arraying for bandwidth enhancement; among other innovations. The subsequent sections of this chapter present the improved results derived from these enhancements. Summing it all up, the results obtained through this study clearly establish the suitability of slotted waveguide arrays as viable sensors in contemporary microwave remote sensing applications. Despite the preliminary nature of this research, the compelling findings invigorate further investigations and innovations with slotted waveguide antenna arrays across diverse modern applications.

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5.1 INTRODUCTION

Remote sensing is the process of gathering information about an object without making any sort of physical contact with it [1]. For remote sensing, humans and animals rely on their biological senses. Mechanical devices, on

the other hand, employ a slew of specialized instruments to detect an extensive range of electromagnetic frequencies emitted or reflected by the target. This enables them to collect information about the object. Specifically, the microwave portion of the electromagnetic spectrum holds special significance due to its high atmospheric transmittance and its ability to penetrate dense clouds. These qualities make it highly advantageous for Earth observation regardless of time or weather conditions, rendering it an excellent choice for space-based remote sensing applications [1].

In the present day, remote sensing plays a crucial role in activities, such as weather forecasting, disaster mitigation, ocean monitoring, agricultural yield prediction, and numerous other essential operations [2, 3]. This emphasizes the importance of continuous technological improvement in this field.

Remote sensing techniques have evolved over the years. For instance, creative scanning modes that involve electronically or mechanically manoeuvring the antenna radiation beam for more detailed visualization. To gain a better understanding of target object characteristics, multispectral imaging employs antennas capable of capturing a variety of frequencies of the electromagnetic spectrum. Polarimetry is a powerful new technique for generating highly detailed images which employs antennas with multiple polarization capabilities (HH, VV, VH) [1].

Initially, slotted waveguide antennas were unable to support these techniques, leading recent missions to switch to MPAs due to their better polarization and frequency flexibility. Recent slotted waveguide investigations suggest novel design approaches for dual polarization or full polarimetry [4]. While these types of theoretical designs appear suitable for modern remote sensing [5, 6], none have been tested against realworld

deployed antennas. This chapter compares a proposed design to an antenna currently operational to identify any discrepancies.

5.2 OBJECTIVE

This chapter compares a newly designed slotted waveguide array antenna with an established remote sensing antenna deployed on an active mission. By closely analyzing different parameters, the study seeks to pinpoint the differences between the two antennas. The gold standard for performance is the advanced dual-frequency synthetic aperture radar (DF-SAR) used in Ch-II, which sets a high-performance benchmark. To facilitate the comparison, a dual-frequency slotted waveguide array antenna (DF-SWA) with dual polarization capability is proposed [1]. The primary goal would be to determine the degree of similarity between the DF-SWA and the DF-SAR antenna's performance. This opens up new avenues for delving deeper into the study of slotted waveguides and for the development of novel polarization or frequency flexible slotted waveguide antenna array (SWAAs) [1].

5.3 SLOTTED WAVEGUIDE ARRAYS: BENEFITS OVER MICROSTRIP ARRAYS

SWAAs have been chosen in this study as they are renowned for their long-distance point-to-point connectivity. Slotted waveguides find particular utility as transceivers in radar systems aboard aircraft or spacecraft due to their conformability to non-linear mounting surfaces, such as aircraft wings or underbellies. Because they are constructed with traditional waveguides, these antennas have high efficiency and energy handling capabilities. This also allows for the integration of the powerfeeding network within the antenna structure itself, thereby enhancing its compactness. However, their inherent resonant nature limits them to narrow-band operations, a constraint

which has been addressed in many contemporary studies [7, 8, 9, 10 and 11].

Waveguide-based antennas, such as slotted waveguide arrays, hold a significant edge over microstrip patch antennas due to their lower loss per unit length at a given frequency. Microstrip lines exhibit approximately 100 times greater transmission loss than waveguides, despite their shorter lengths [12]. Consequently, slotted waveguide arrays, with waveguidebased power distribution networks, exhibit markedly reduced power losses in comparison to microstrip patch antennas. Furthermore, waveguides surpass microstrip lines in power handling, as the latter are also susceptible to dielectric breakdown at higher power levels. Dielectric and conductor losses plague microstrip patch antennas, hampering efficiency, whereas waveguides shine in efficiency.

5.4 ANALYSIS OF LAYOUT AND PERFORMANCE

5.4.1 DUAL FREQUENCY-SAR ANTENNA OF CH-II

Ch-II's DF-SAR antenna is a dual-layered MSA with dual-polarization and dual-frequency (L-Band at 1.25 GHz and S-Band at 2.5 GHz) capabilities. To achieve a compact design, L-Band patches and S-Band patches, along with their respective power networks, are organized across multiple substrate layers. It has an approximate size of 1.35 m × 1.1 m and weighs in at 3.6 kg. Figure 5.1, Ref. [13] displays the antenna's schematic diagram [1].

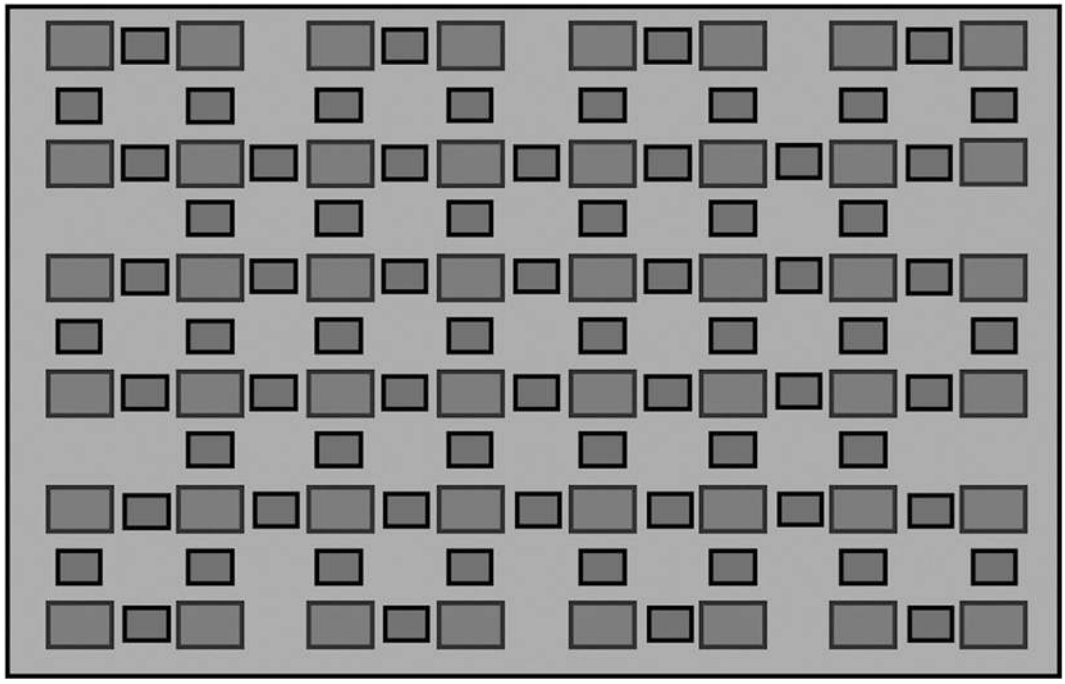

FIGURE 5.1 Layout diagram of Ch-II's DF-SAR antenna.

The antenna operates with linear and circular polarization in both L and S bands, either individually or simultaneously. In circular polarized mode of operation, it gives an axial ratio better than 2 dB. In linear polarized mode of operation, it has cross polar isolation better than 30 dB.

5.4.2 DUAL-FREQUENCY SWA: CONVENTIONAL DESIGN

To match the performance of the DF-SAR antenna, a dual-frequency SWA capable of dual LP has been designed at the same frequencies for a thorough analysis and performance evaluation [1]. Power is fed from opposite ends of a single, compact antenna that combines both L and S band arrays where the array elements are interleaved. The array has a total of 120 radiating elements. Horizontally polarized broadwall shunt slots are used for the 2.5 GHz S-Band array. WR650 waveguide with a cross-section of 165.1 mm × 41.28 mm has been used. Using vertically polarized rotated slots in the narrow wall of a rectangular waveguide, the L-Band array operates at 1.25 GHz. WR340 waveguide with cross-section of 86.36 mm ×

43.18 mm has been used. In the L-Band configuration, lower profile waveguides were used to reduce the spacing between two waveguides within the planar array. This improves the side lobe reduction of the radiated emission at either frequency. Figure 5.2A provides insights into the array's characteristics. The overall layout of the array is depicted by Figure 5.2B. Figure 5.2C depicts 3D view of the interspersed structure.

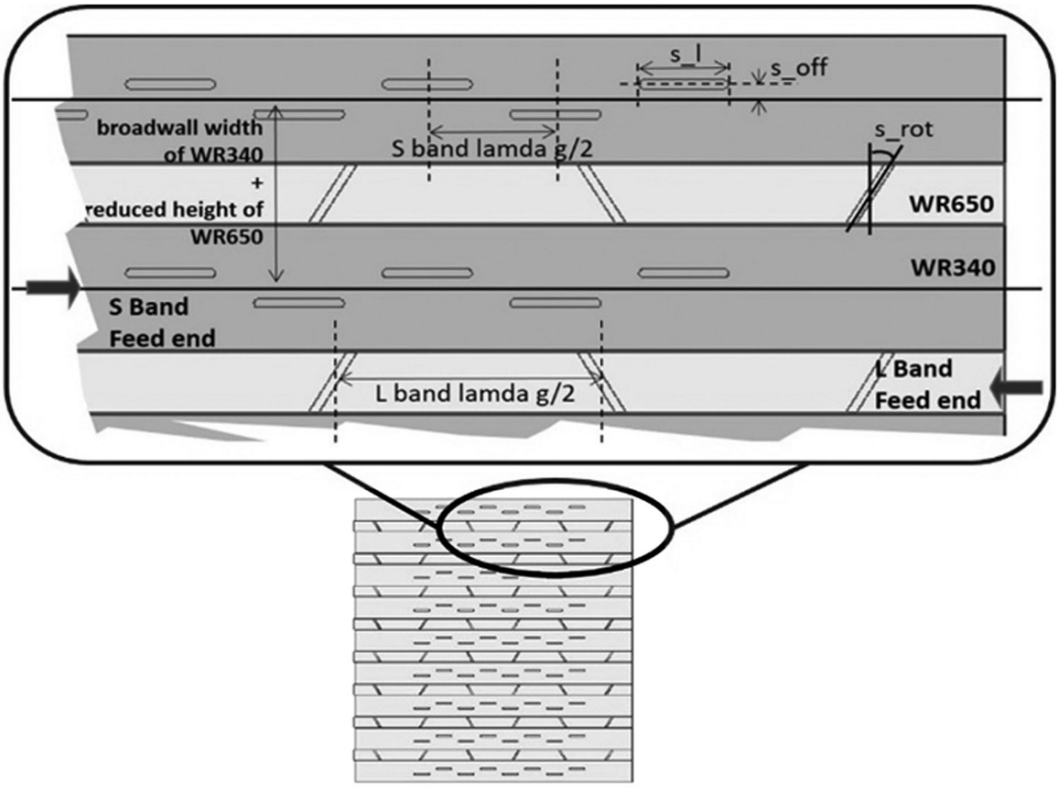

FIGURE 5.2A Array characteristics.

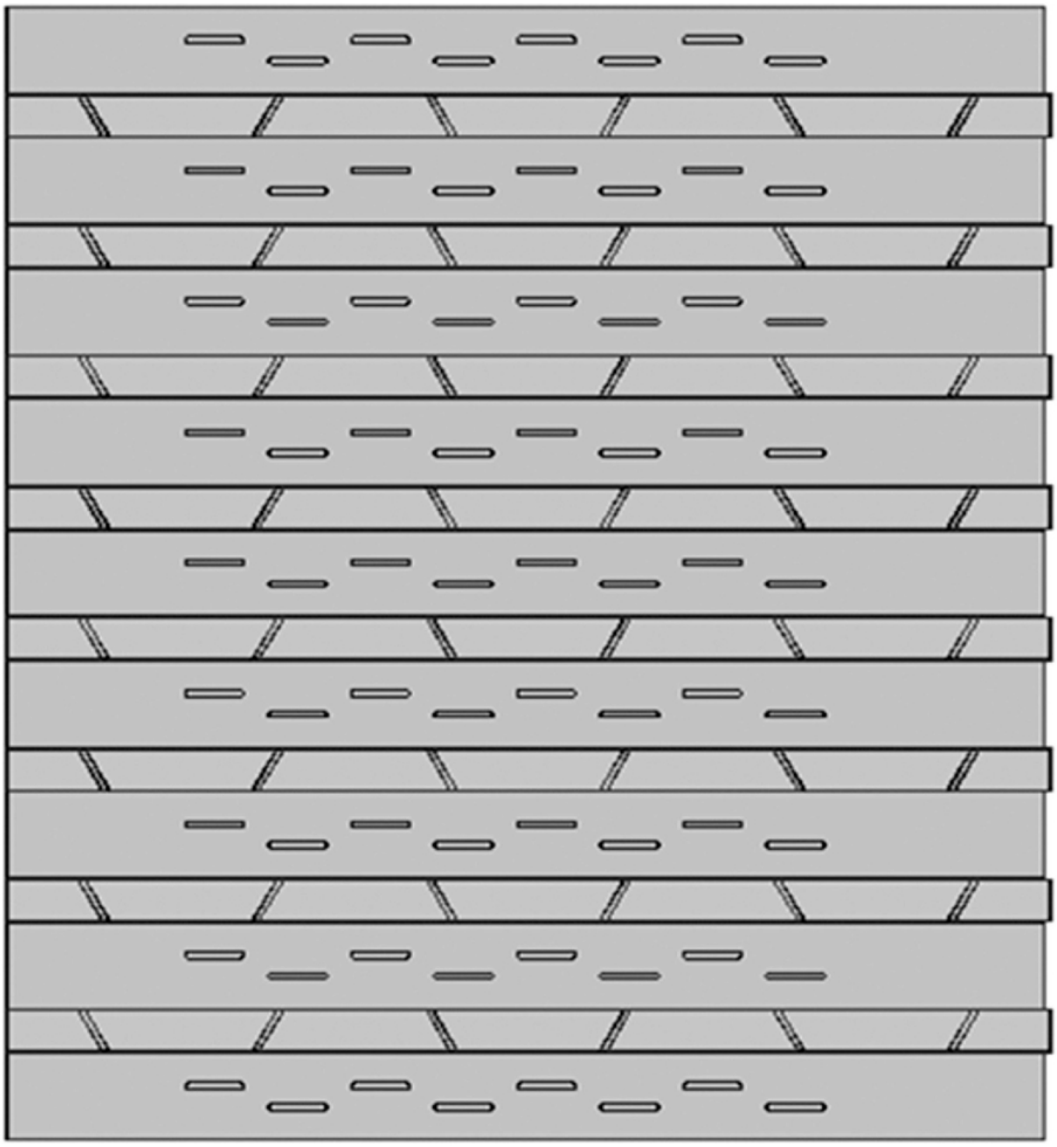

FIGURE 5.2B Layout diagram of dual-polarized dual-frequency slotted waveguide array antenna.

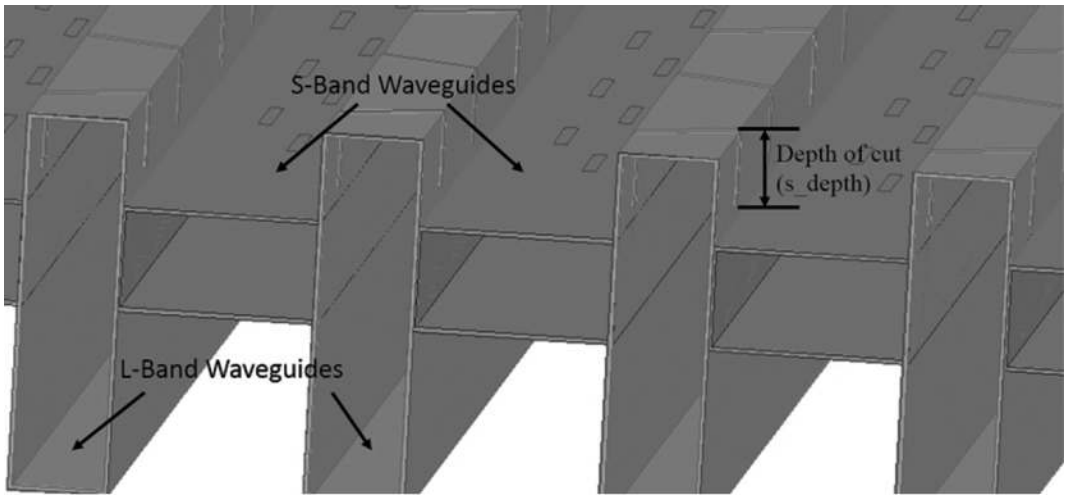

FIGURE 5.2C 3D view of waveguides in the L and S-Band.

5.4.3 OBSERVATIONS: CONVENTIONAL DESIGN

A meticulous systematic analysis and performance assessment has been carried out between the DF-SAR antenna and the conventional dualpolarized DF-SWA antenna by the authors which is available in Ref. [1]. A detailed summary of the performance is outlined in Table 5.1.

TABLE 5.1 Summary of Performance [1].

Parameter	**DF-SWA Antenna**		**DF-SAR Antenna**	
	L-Band (1.25 GHz)	**S-Band (2.5 GHz)**	**L-Band (1.25 GHz)**	**S-Band (2.5 GHz)**
Maximum gain	22 dBi	23.66 dBi	22 dBi	25 dBi
HPBW	12.8° × 12.9°	4.8° × 8.3°	9.2° × 11.2°	4.6° × 5.6°
Bandwidth	50 MHz	110 MHz	75 MHz	180 MHz
Cross-polarization isolation	60 dB	28 dB	30 dB	30 dB
SLR	15 dB	9 dB	Data unavailable	Data unavailable

The preliminary findings presented in Table 5.1 offer some noteworthy observations. When operating in the linear polarized mode, the standard SWA antenna demonstrated performance levels that were very close to those of the DF-SAR antenna. Yet, performance disparities were noted in certain parameters. These findings and possible solutions are summarized as follows:

1. It may be observed that the side lobe reduction (9 dB at S-Band) achieved through the conventional design falls short of accepted levels. This outcome can be attributed to aperture blockage, an effect stemming from the utilization of interleaved S and L band arrays, thereby resulting in an increased separation distance between the two arrays. It is possible to reduce the separation by incorporating ridged waveguides [24] with narrower broad wall width instead of the standard waveguide.
2. The incorporation of non-uniform aperture excitation for the slots, employing distribution profiles such as, Taylor, Chebyshev, or binomial distributions [22, 25], holds promise in further diminishing the side lobe levels to more desirable thresholds.
3. Frequency achieved by the conventional design is limited. Strategic implementation of sub-arraying techniques can help substantially improve the frequency.

5.4.4 DUAL-FREQUENCY DUAL-POLARIZED SLOTTED WAVEGUIDE ARRAY: ENHANCED DESIGN

The enhancements proposed above are incorporated into the second iteration of the design.

1 Ridged waveguides:

In the second iteration of the design, a single ridged WR229 waveguide (ridge dimensions: 20 mm × 10 mm) has been used for the S-Band instead of WR340. This reduces separation distance between adjacent arrays. Ridged waveguide parameters are enumerated in Table 5.2.

TABLE 5.2 Ridged Waveguide Parameters. ⏎

Design Parameter	**Conventional Design Enhanced Design**	**Size Reduction**
Waveguide: S-Band	WR340 Single ridged WR229	–
Inner dimensions	86.36 mm × 43.18 mm 58.166 mm × 29.083 mm	48%
Guided wavelength (λg)	166.84 mm 144 mm	15.86%
Antenna size	1 m × 1.1 m 0.92 m × 1.04 m	8.7%

2 Non-uniform aperture distribution:

Radiation pattern synthesis and side lobe reduction necessitate accurate determination and control of the displacement of radiating slots from the waveguide centerline. Uniform distribution typically yields a 13 dB SLL.

Well-established optimization methods like Woodward sampling, Chebyshev distribution, Taylor distribution, and so forth, determine distribution coefficients, which when applied to the normalized conductance equation, furnishes slot displacement values based on the linear array's slot count. Here, Chebyshev distribution is employed to ascertain slot offsets [25] and the resultant values are incorporated into the enhanced design and enumerated in Table 5.3.

TABLE 5.3 Non-uniform Slot Displacements for SLL Reduction.

Slot Displacement (mm) Slot	1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6	Slot 7	Slot 8
Uniform distribution	10.46							
Chebyshev distribution	6.92	8.61	9.9	10.61	10.61	9.9	8.61	6.92

3 Sub-arrays:

Enhancement of antenna bandwidth can be achieved by reducing the reactive component of input admittance across the frequency range of interest. Through meticulous selection of slot count in the array, this reactive component can be nearly eliminated within the target frequency range, leading to an expanded bandwidth [8]. For applications demanding larger arrays, the most efficient approach for enhancing bandwidth involves partitioning the array into smaller sub-arrays, each with its dedicated power feeding network. In this design, the eight-element S-band array has been divided into two sub-arrays, each comprising four elements. The implementation is illustrated in Figure 5.3.

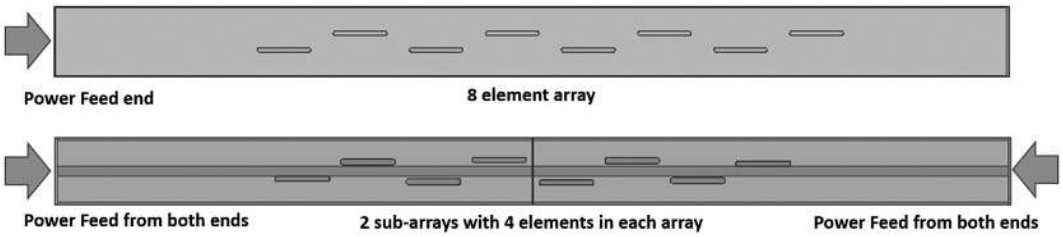

FIGURE 5.3 Sub-array implementation at S-Band.

Finally, the schematic diagram of the enhanced antenna after implementation of all proposed changes is shown in Figure 5.4.

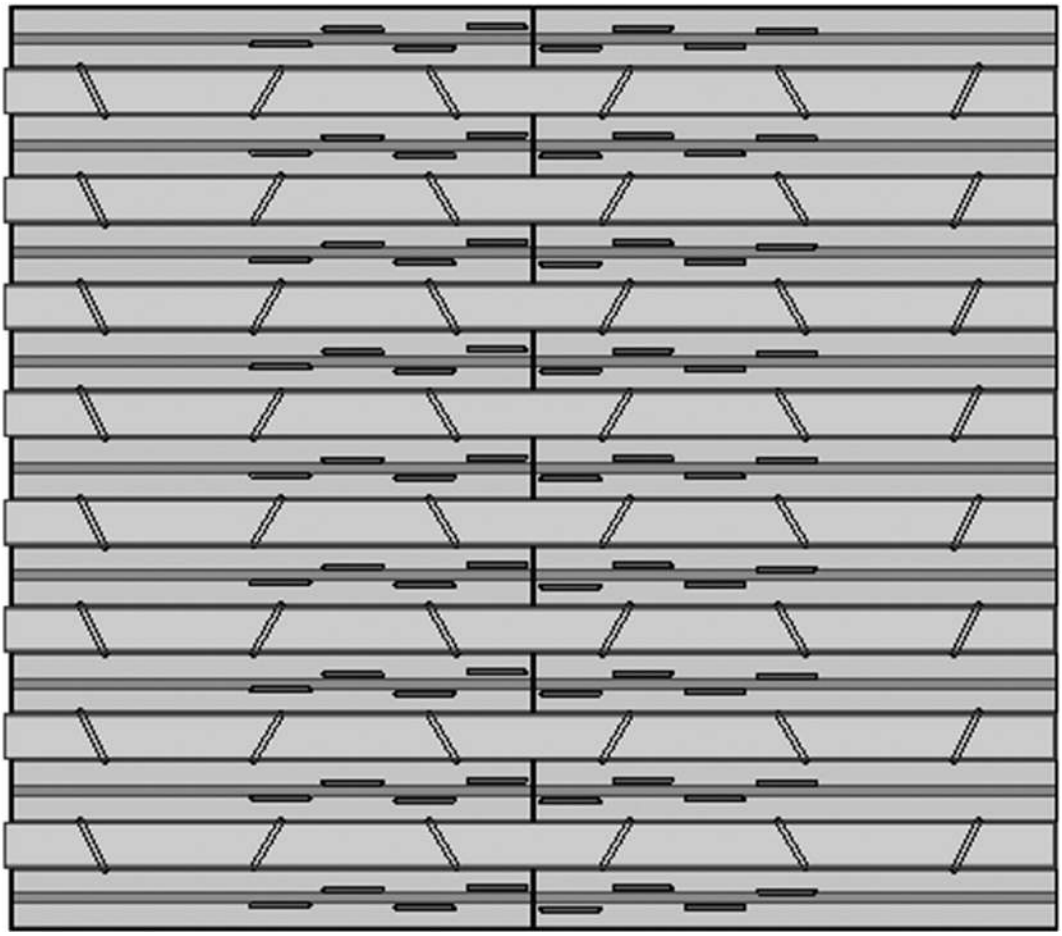

FIGURE 5.4 Layout diagram of enhanced antenna.

5.4.5 PERFORMANCE ANALYSIS: ENHANCED DESIGN

Figures 5.5A and B depict the enhanced design's radiation pattern attributes at L-Band and frequency, respectively.

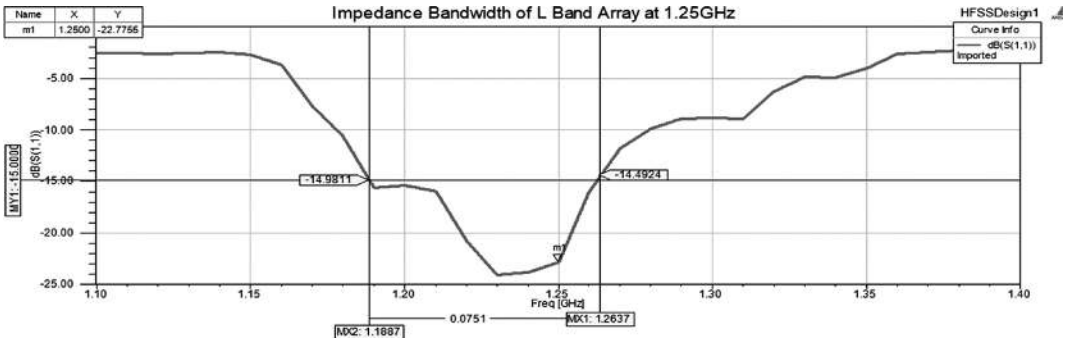

FIGURE 5.5A Frequency of enhanced antenna at L-Band.

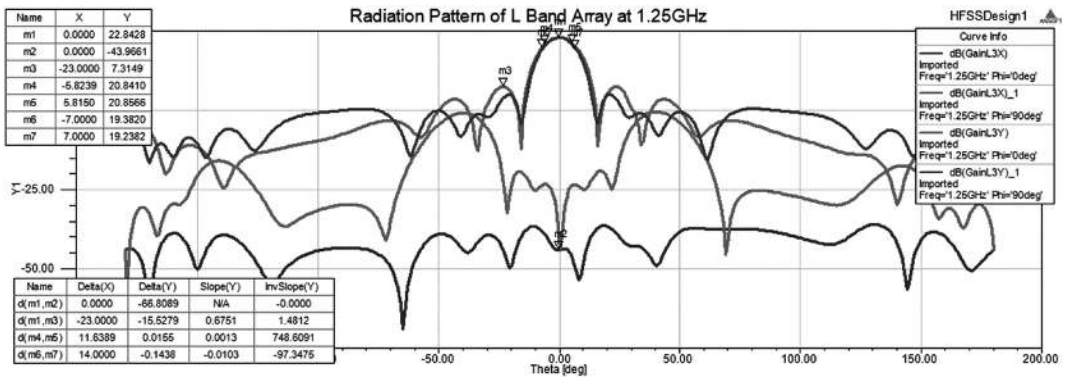

FIGURE 5.5B Radiated emission of enhanced antenna at L-Band.

The L-Band array's impedance bandwidth has grown from its previous value of 50 MHz to approximately 75 MHz. The highest gain manifested has increased to 22.8 dBi with SLR greater than 15.5 dB and cross-polarization isolation greater than 60 dB. The array's HPBW is now 11.6° × 14°.

Likewise, Figures 5.6A and B display the radiation pattern traits at S-Band and the Frequency.

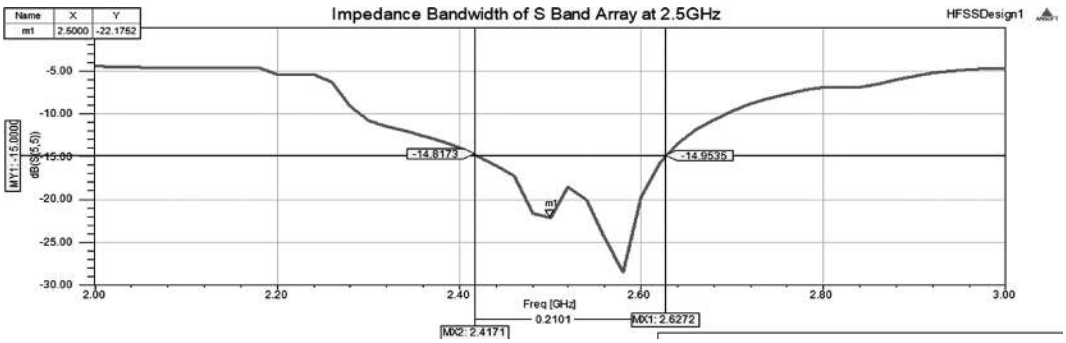

FIGURE 5.6A Frequency of enhanced antenna at S-Band.

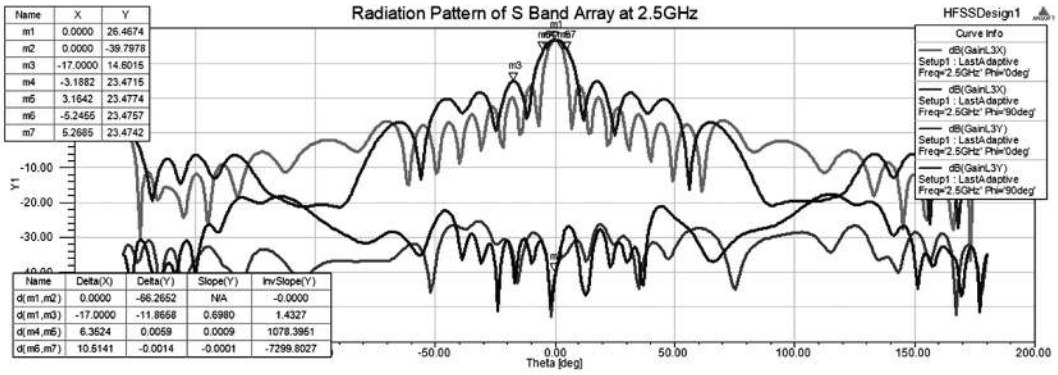

FIGURE 5.6B Radiated emission of enhanced antenna at S-Band.

After the implementation of the sub-array concept, the frequency of the S-Band array has increased significantly to 210 MHz (compared to the 110 MHz earlier). The gain output has increased significantly to 26.47 dBi as compared to the earlier value of 23.66 dBi with side lobe reduction greater than 12 dB now (as compared to 9 dB earlier) with cross-polarization isolation higher than 60 dB. The HPBW has degraded slightly and is now 6.3° × 10°.

A detailed parametric comparison and performance assessment between the three designs: DF-SAR antenna, conventional slotted waveguide array and the enhanced slotted waveguide array is presented in Table 5.4.

TABLE 5.4 Comparative Analysis Between Three Designs. ⏎

Parameter	DF-SAR Antenna		Conventional Design		Enhanced Design	
	L-Band	S-Band	L-Band	S-Band	L-Band	S-Band
Maximum gain	22 dBi	25 dBi	22 dBi	23.66 dBi	22.8 dBi	26.47 dBi
HPBW	9.2° × 11.2°	4.6° × 5.6°	12.8° × 12.9°	4.8° × 8.3°	11.6° × 14°	6.3° × 10°
Bandwidth	75 MHz	180 MHz	50 MHz	110 MHz	75 MHz	210 MHz
Cross-polarization isolation	30 dB	30 dB	60 dB	28 dB	60 dB	60 dB
SLR:	Data unavailable	Data unavailable	15 dB	9 dB	15.5 dB	12 dB

5.5 FUTURE SCOPE

Although the very detailed parameter wise comparative analysis shown in Table 5.4 shows that performance levels similar to the DF-SAR antenna can be achieved by SWAA; it is possible when operating in linear polarization. Despite the preliminary nature of this research, the intriguing findings call for further investigations with SWAA, particularly for implementation of circular polarization. Following are some possibilities for implementation of circular polarization in the future:

1. In order to produce CP in slotted waveguide arrays, compound slots as opposed to resonant slots [17, 18], parasitic dipole components [19], use of rectangular cavities with power feed from the slot array [20] can all be used. Further research may make use of these methods.

2. To achieve circular polarization, another viable option that merits more research is to use SRRs as the radiating slot [21].
3. Although sidelobe reduction with non-uniform distribution was achieved, a novel method of sidelobe reduction by utilizing a waveguide with stepped sidewalls [23] can be studied in the future.
4. Bandwidth enhancement has been achieved through sub-arraying technique in this study. The corresponding author of this study has also previously written about another bandwidth improvement method [7], which can be used in the next design iteration.
5. This design is intended to be used as a sensor for radars. A radar is made up of several discrete systems that work together, each with multiple sub-components. Each of these subsystems must be tested separately. Since the design being presented here is meant to be utilized as a sensor for radars, it is necessary to test the design's general antenna properties in order to evaluate it. Network analyzers and anechoic chambers make this feasible. A scaleddown version (small array) will be fabricated, and its frequency attributes will be tested using a network analyzer.

5.6 CONCLUSION

In conclusion, this investigation affirms that SWAs hold promise for microwave remote sensing applications, provided slight augmentations or the adaption of alternative scanning techniques (e.g., conical scanning) to accommodate polarization-sensitive measurements are implemented. The impending integration of these refinements by the authors in the forthcoming design iteration underscores their commitment to advancing this field. The promising results of this preliminary investigation clearly establish SWAs as viable detectors in modern remote monitoring purposes,

thereby beckoning for deeper and more comprehensive explorations into this domain.

KEYWORDS

- **antenna bandwith**
- **aperture radar**
- **electromagnetic spectrum**
- **microstrip**
- **polarization**
- **remote sensing**
- **slotted waveguide antenna arrays**

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CHAPTER 6
Missing Cell Defect Analysis of Reversible 1-Bit Magnitude Comparator

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ABSTRACT

Complementary metal oxide semiconductor (CMOS) technology has established the fabrication of processors with less area and power dissipation with high-speed performance. However, this technology causes heat and energy dissipation that can cause hurdles in the processor's speed. Irreversible computation in CMOS causes heat and energy dissipation. Solution to this heat and energy dissipation is to use reversible logic instead of the conventional irreversible logic synthesis. In this chapter, a reversible technology-based 1-bit comparator design is proposed. Quantum-dot cellular automata (QCA) nanotechnology is used for the implementation of proposed design. QCA designer tool is used for device-level implementation. The proposed reversible comparator is also implemented at the logic level using Verilog hardware description language (HDL) to compare the results with device-level implementation. The synthesis and simulation are carried out using the Xilinx ISE tool. Further, the missing

cell defect analysis of the proposed circuit is carried out and presented in this chapter.

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6.1 INTRODUCTION

The current complementary metal oxide semiconductor (CMOS) technology is ruling the semiconductor industry since many decades. It is irreversible in nature which means the bits get erased during the computation. This bit erasing process causes energy dissipation in the circuit, and hence in the system. The dissipated energy is equal to KTln2, where K is Boltzmann's constant in joule per kelvin and T is the temperature in kelvin [1]. This heat dissipation is one of the hurdles faced by the processor in achieving speed. This problem can be avoided if the circuit and system is based on reversible computation. Reversible logic consists of equal number of inputs and outputs [2]. Reversible computation is also area and power efficient. So, wide applications in the area of low-power digital logic circuit, Internet of Things (IoT), and quantum computing are possible using this technology [3]. Quantum-dot cellular automata (QCA) can be used for the device-level implementation of reversible gates and circuits [4]. Therefore, the proposed design consisting reversible gates are implemented using QCA.

In this chapter [5], the QCA-based ultra-dense comparator design using MV32gate is presented. In the literature, only irreversible QCAbased comparator designs are available. In Ref. [6], N-bit reversible comparator is proposed. Low-power reversible comparator design is available in Ref. [7].

N-bit binary tree structure based comparator with a low latency is proposed in Ref. [8]. In Ref. [6, 7 and 8], only gate level implementations are available. No one has described and implemented design at the device-level

In this chapter, QCA technology based reversible gates are implemented. QCADesigner simulator tool is used for all simulations throughout this chapter. Furthermore, 1-bit reversible magnitude comparator design is proposed. Both the implementations, device-level and logic-level are demonstrated in this chapter. QCADesigner and Xilinx ISE 13.1 tools are used for the device-level and logic-level implementations, respectively. The calculations for the performance parameters of the proposed comparator design, namely quantum cost, garbage output, and energy dissipation are carried out. Further, the single missing cell defect analysis for reversible gates used for the implementation of the proposed design is carried out using extensive simulation and presented in this chapter. Afterward, the effect of these defects on the proposed comparator is presented.

This chapter is presented as follows: significance of reversible circuits, reversible terminologies, and background of QCA technology is presented in Section 6.2 The implementation of reversible gates is described in Section 6.3. Device-level implementation of the proposed comparator is presented in Section 6.4 while the logic-level implementation is presented in Section 6.5. The defect analysis is presented in Section 6.6. Section 6.7 presents a comparative analysis. Section 6.8 concludes this chapter.

6.2 FUNDAMENTALS

6.2.1 REVERSIBLE CIRCUITS

Following are the terminologies of reversible circuits:

1. Logical reversibility: In logical reversibility, bits are preserved, that is, number of inputs and outputs are equal.
2. Physical reversibility: In physical reversibility, inputs and outputs are interchangeable.
3. Garbage output (GO): To maintain the logical reversibility, inputs and outputs are equal. The unused output to do so is known as garbage output.
4. Quantum cost (QC): The number of gates or primitives used to build a reversible circuit is known as quantum cost.

6.2.2 QUANTUM-DOT CELLULAR AUTOMATA (QCA)

QCA technology cell contains four or six quntum dots. QCA gates consists of array of cells or specific arrangements of cells to form respective logic. Each QCA cell consists of two highly free electrons as shown in Figure 6.1. These two free electrons are always set diagonally to each other because of coulombic repulsion [4]. The cell polarization is decided depending upon the electrons position as "−1" or "+1" as shown in Figure 6.2. It is then considered as binary logic "0" and "1."

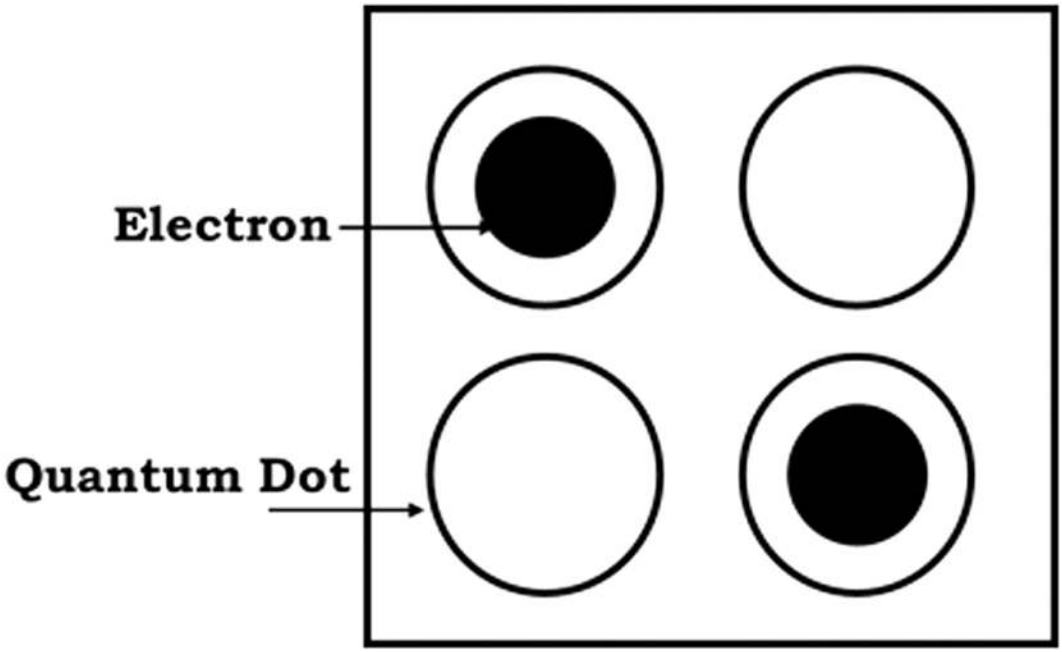

FIGURE 6.1 Quantum-dot cellular automata cell.

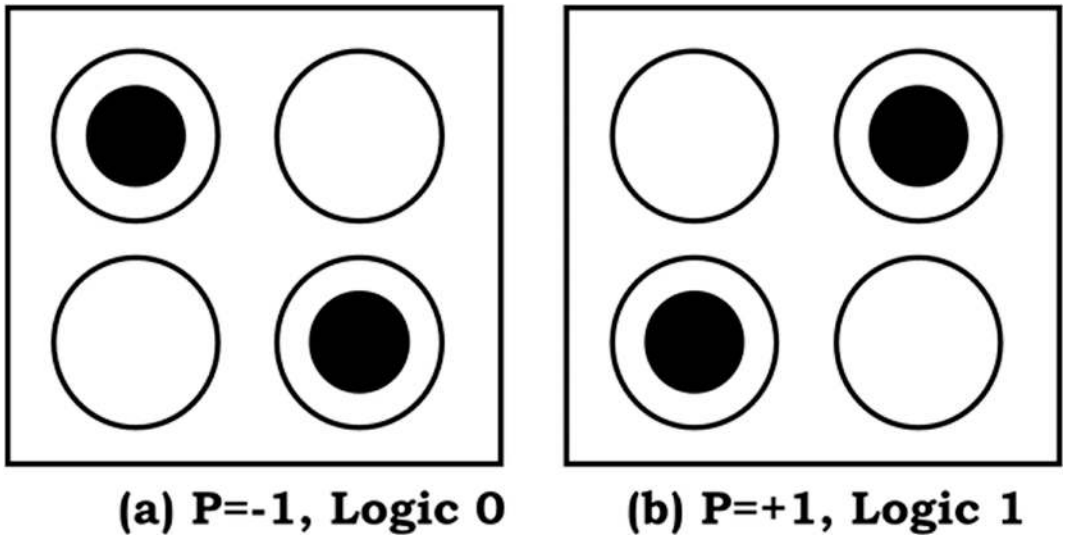

FIGURE 6.2 QCA cell having different polarization (A) P = −1 and (B) P = +1.

6.2.3 MAJORITY VOTER (MV)

Majority voter is main logic gate in QCA. This five cell configuration shown in Figure 6.3 gives the output as a majority of three inputs. The Boolean equation is given in Equation 6.1.

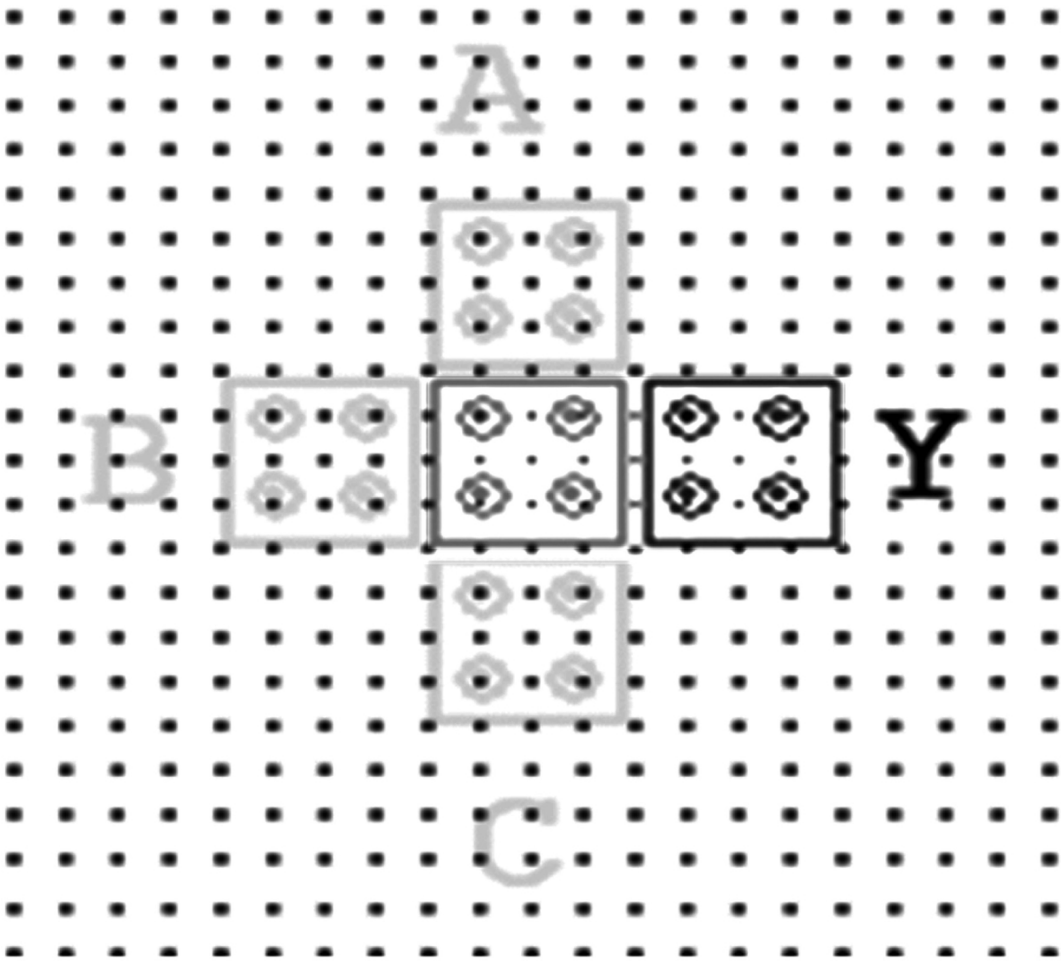

FIGURE 6.3 Majority voter (MV).

$$Y = (A \times B)|(B \times C)|(C \times A) \tag{6.1}$$

Where Y is the output and A, B, and C are inputs of MV gate.

6.3 IMPLEMENTING THE REVERSIBLE GATES

The proposed comparator design is a combination of reversible gates Fredkin and Feynman. First MV using QCA is implemented and the reversible gates are then implemented using MVs. QCADesigner [9], an open source tool is used for implementation.

QCADesigner's bistable approximation engine is selected to simulate all the reversible gates and proposed circuit. The simulation parameters are listed in Table 6.1. Other parameters are kept as default.

TABLE 6.1 Simulation Parameters.

Parameter	Value
Size of a cell	18 nm × 18 nm
Distance between two cells	2.5 nm
Diameter of a dot	5 nm
Distance between two dots	9 nm
Effective radius	65 nm
High clock	9.8e-22
Low clock	3.8e-23
Clock amplitude factor	2

6.3.1 FREDKIN GATE

Fredkin reversible gate [10] consists of three inputs and outputs. Outputs of Fredkin gate are P = A, Q = A'B+AC, and R = AB+A'C. Figure 6.4 shows the block diagram of the Fredkin gate.

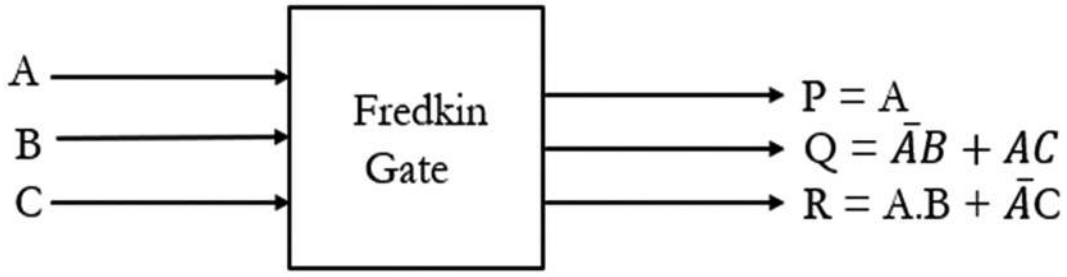

FIGURE 6.4 Fredkin gate.

The Fredkin gate implementation based on QCA is shown in Figure 6.5. Six QCA MVs and one inverter are used for the implementation of Fredkin gate. MV can be made as OR and AND gate by keeping its one of the inputs at +1 and −1, respectively.

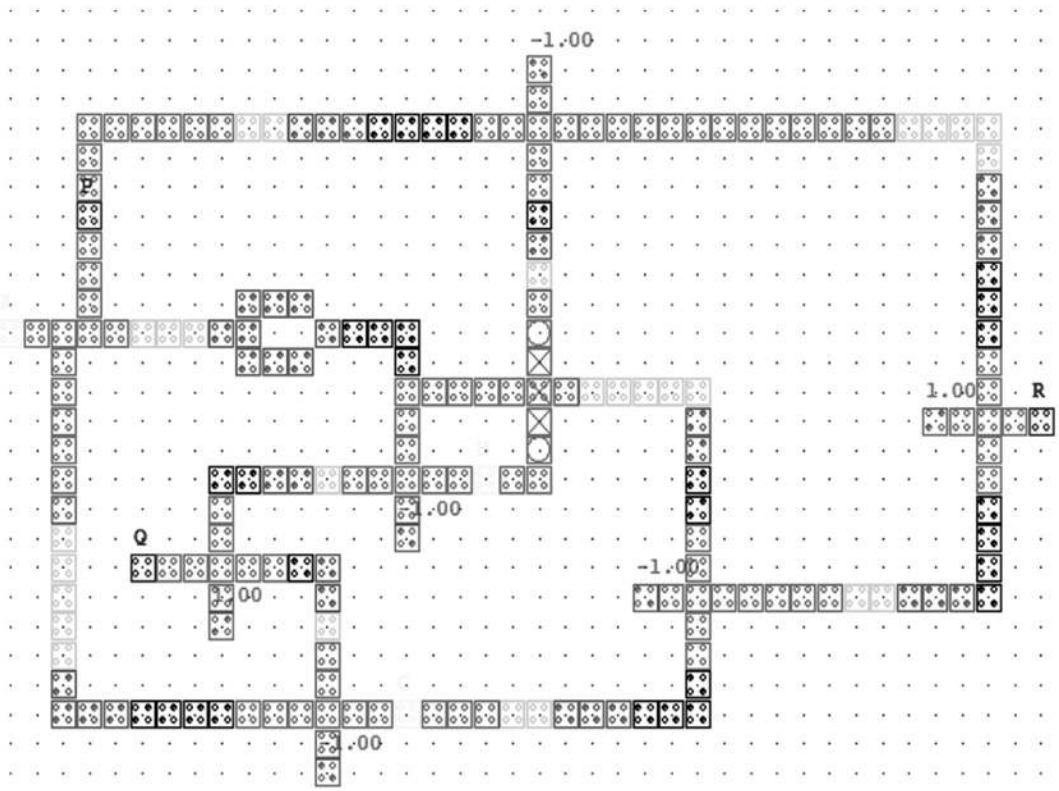

FIGURE 6.5 Quantum-dot cellular automata implementation of Fredkin gate.

The simulation result of Fredkin gate is shown in Figure 6.6. It is observed from the simulation results shown in Figure 6.6. that the outputs P = A, Q = A'B+AC, and R = AB+A'C are properly obtained.

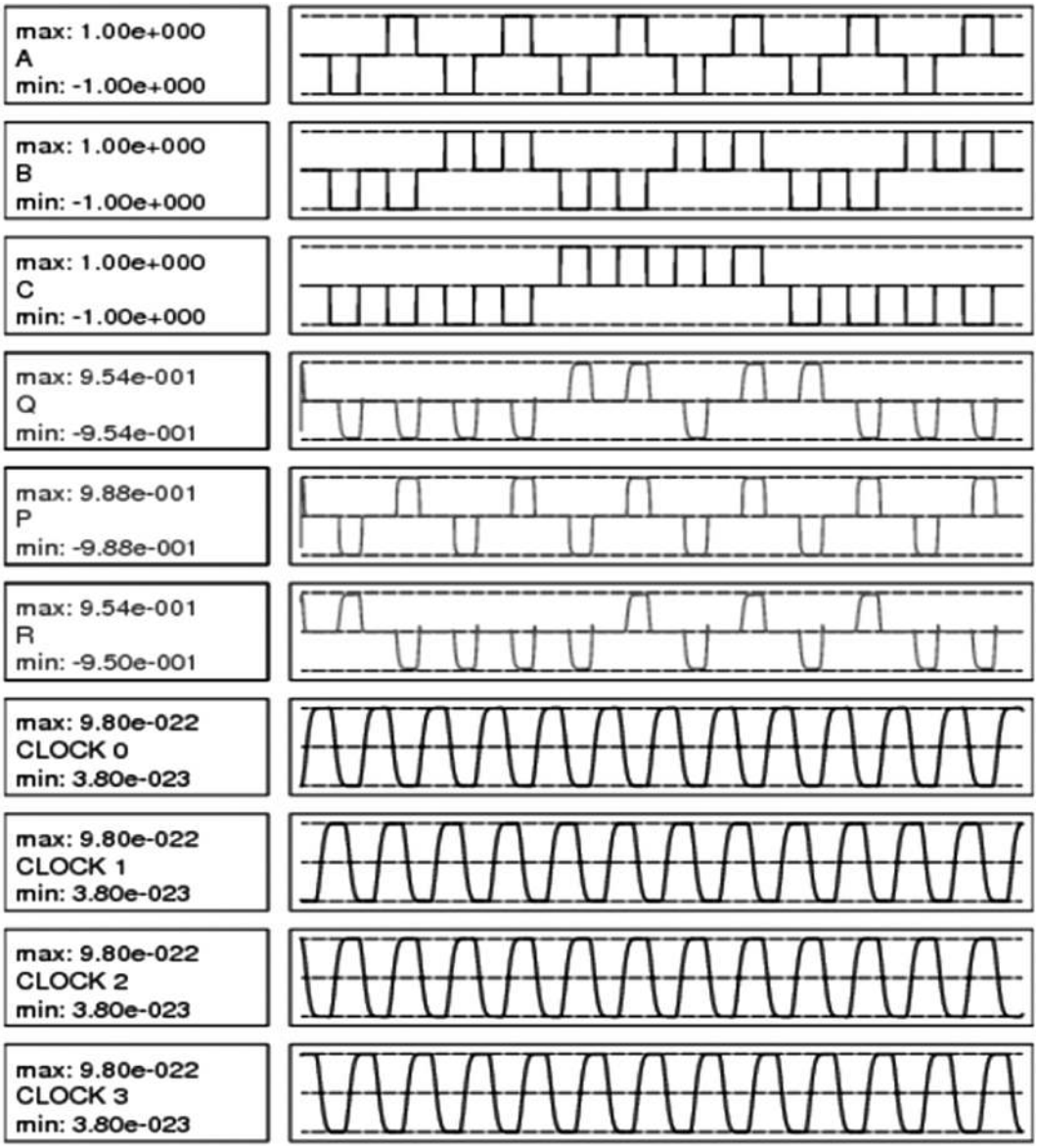

FIGURE 6.6 Simulation result of Fredkin gate.

6.3.2 FEYNMAN GATE

Feynman reversible gate has two inputs and outputs. It implements outputs P = A, Q = A'B+AB'. The block diagram of the Feynman gate is shown in Figure 6.7.

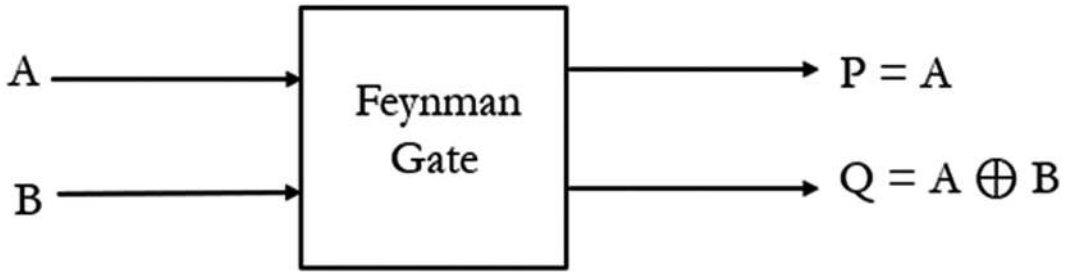

FIGURE 6.7 Feynman gate.

QCA implementation of Feynman gate is shown in Figure 6.8. It consists of three QCA MVs and two inverters.

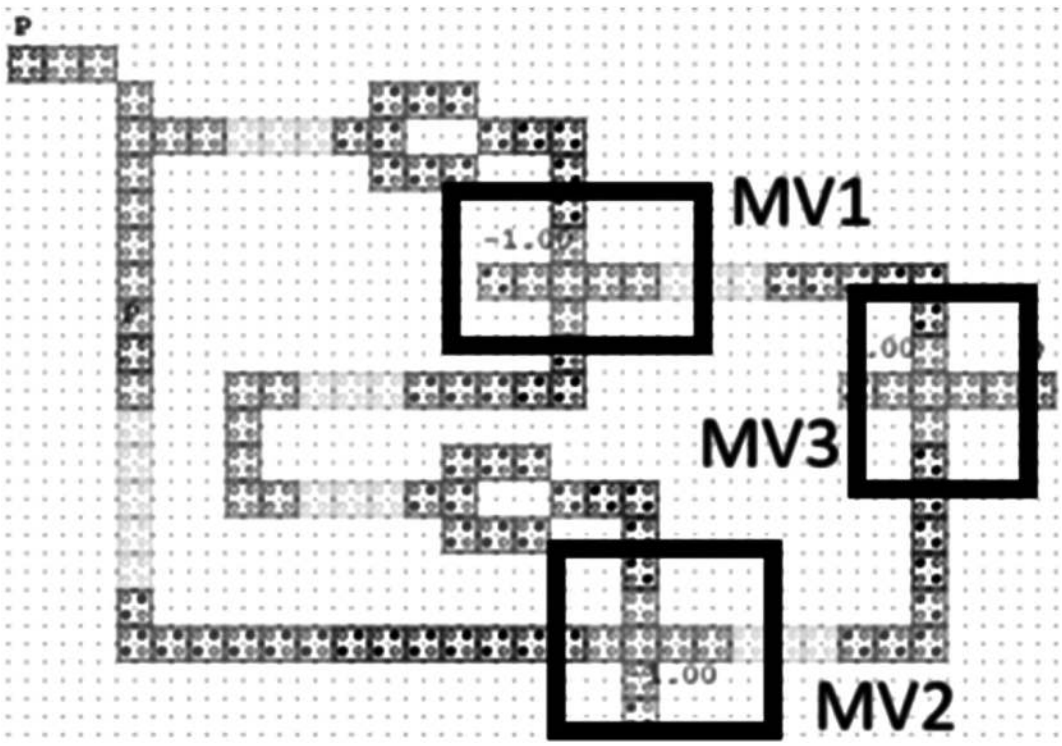

FIGURE 6.8 Quantum-dot cellular automata implementation of Feynman gate.

Simulation result of Feynman gate is shown in Figure 6.9. From Figure 6.9 it is observed that the outputs P and Q are obtained properly. Two clock cycle delay in the output Q is observed in Figure 6.9. This delay occurs in the output because of internal clocking sequence of QCA.

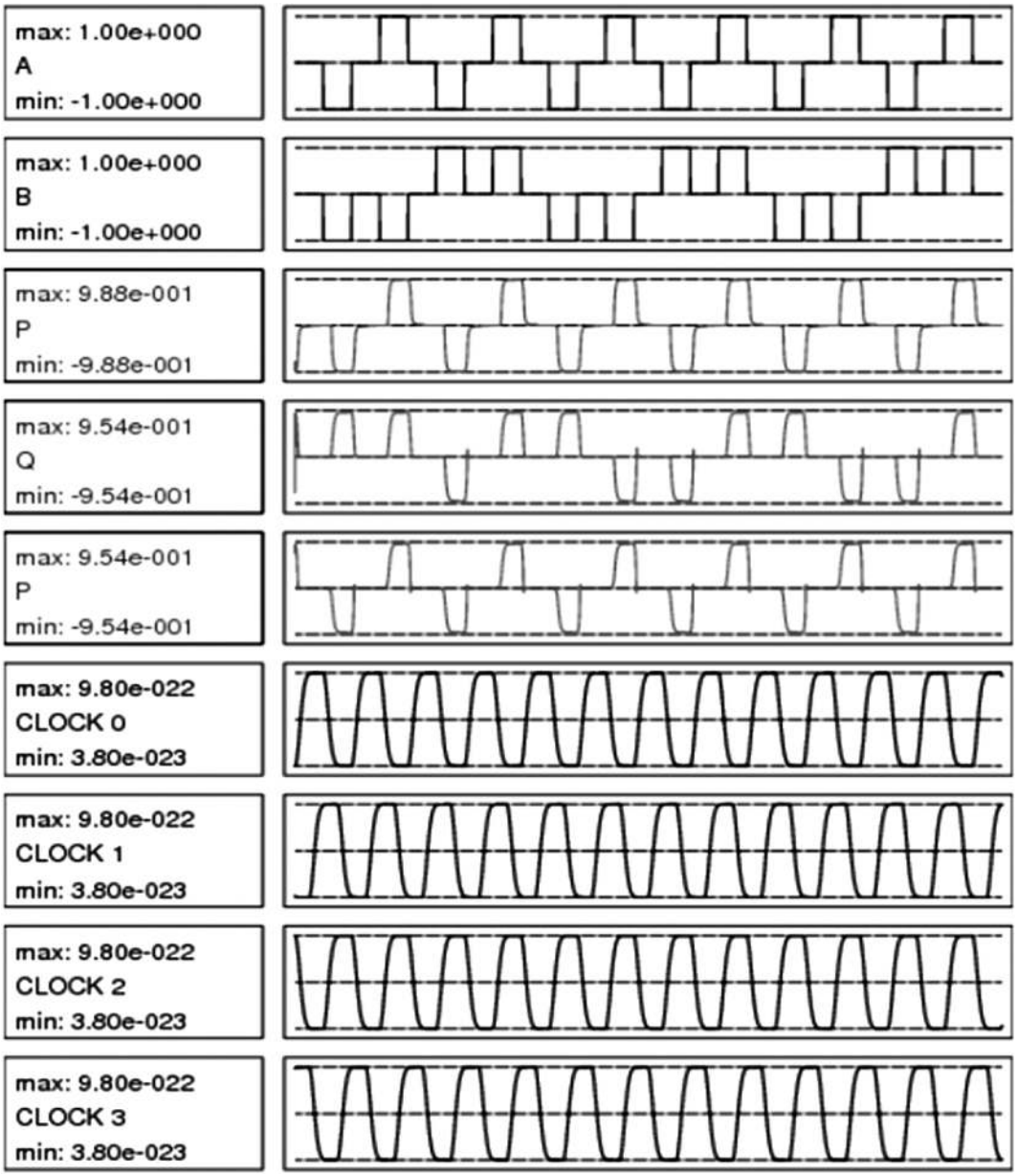

FIGURE 6.9 Simulation result of Feynman gate.

6.4 DEVICE-LEVEL IMPLEMENTATION

In this section, implementation of 1-bit comparator design based on reversible gates is presented. 1-bit comparator has two inputs and three outputs. Three outputs are A. $\overline{B}$ for A > B, $\overline{A}$ B for A < B, and $A \oplus B$ for A = B as shown in Figure 6.10.

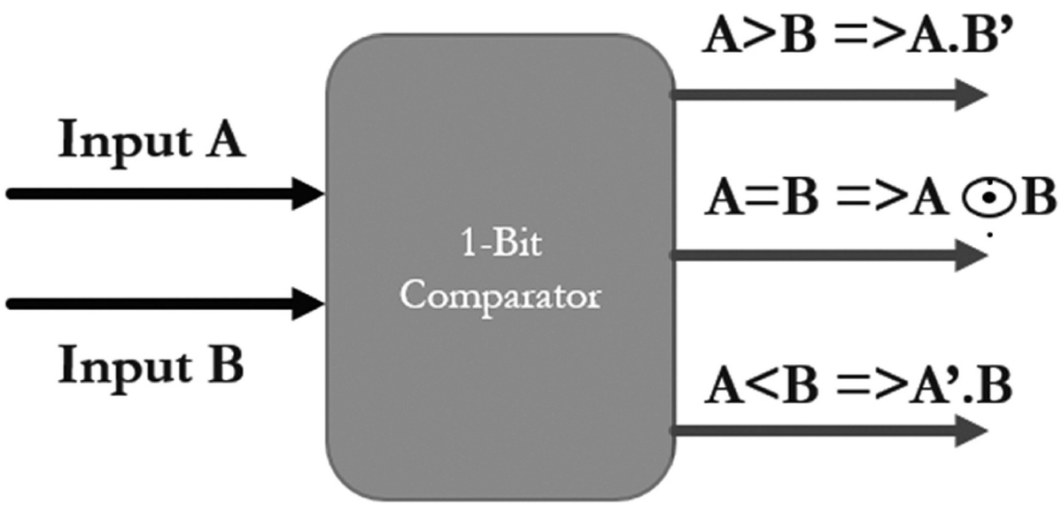

FIGURE 6.10 1-bit comparator.

For the implementation of comparator shown in Figure 6.10, two Feynman and one Fredkin gates are used. The block diagram of proposed reversible-based 1-bit comparator is shown in Figure 6.11. Input A and B of comparator are connected to the inputs of Feynman gate. According to the functionality of Feynman gate as shown in Figure 6.7, the outputs are P = A and Q = A'B+AB'.

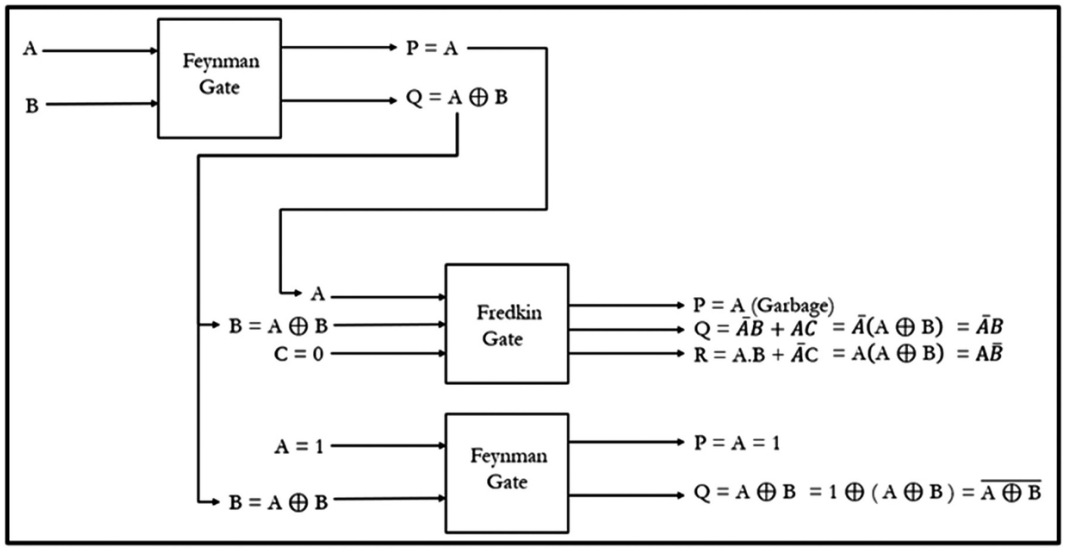

FIGURE 6.11 Single-bit reversible comparator with three inputs and three outputs.

Further, the Feynman gate's outputs P and Q are connected to the inputs A and B of Fredkin gate, respectively. From this Fredkin gate, both the functionalities of the comparator namely A > B and A < B are obtained at its output.

The output Q of the first Feynman gate is connected to the second Feynman gate. The comparator's functionality A = B is obtained at the output of the second Feynman gate. Two GOs are obtained in this design which can be further useful to take other circuit's functionality. In this way, two Feynman and one Fredkin gates form a comparator.

QCA implementation of the proposed 1-bit comparator consisting reversible gates is shown in Figure 6.12. The QC for the proposed design Feynman gate has a QC of 1 and there are two such gates in design. So, 1 × 2 = 2. Similarly, Fredkin's QC is 5 and there is one such gate. So, the total QC of the proposed design is 2+5 = 7.

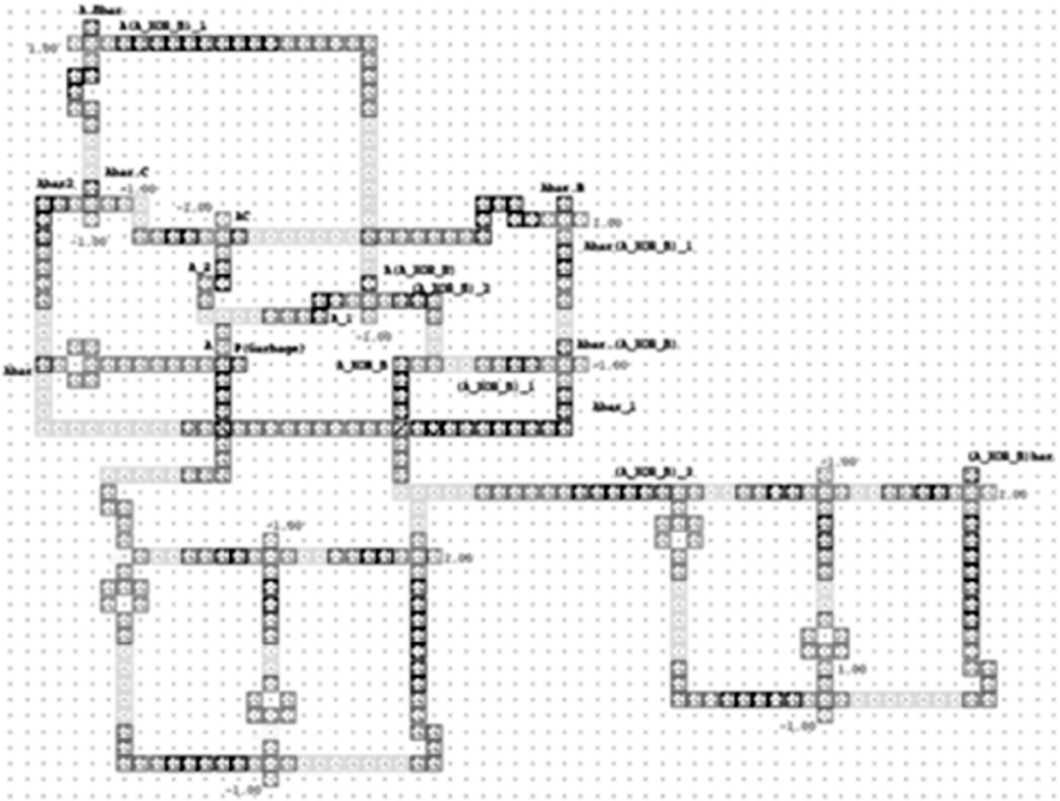

FIGURE 6.12 QCA implementation of proposed single-bit reversible comparator.

The simulation is carried out with the simulation parameters mentioned in Table 6.1. Figure 6.13 shows the results obtained.

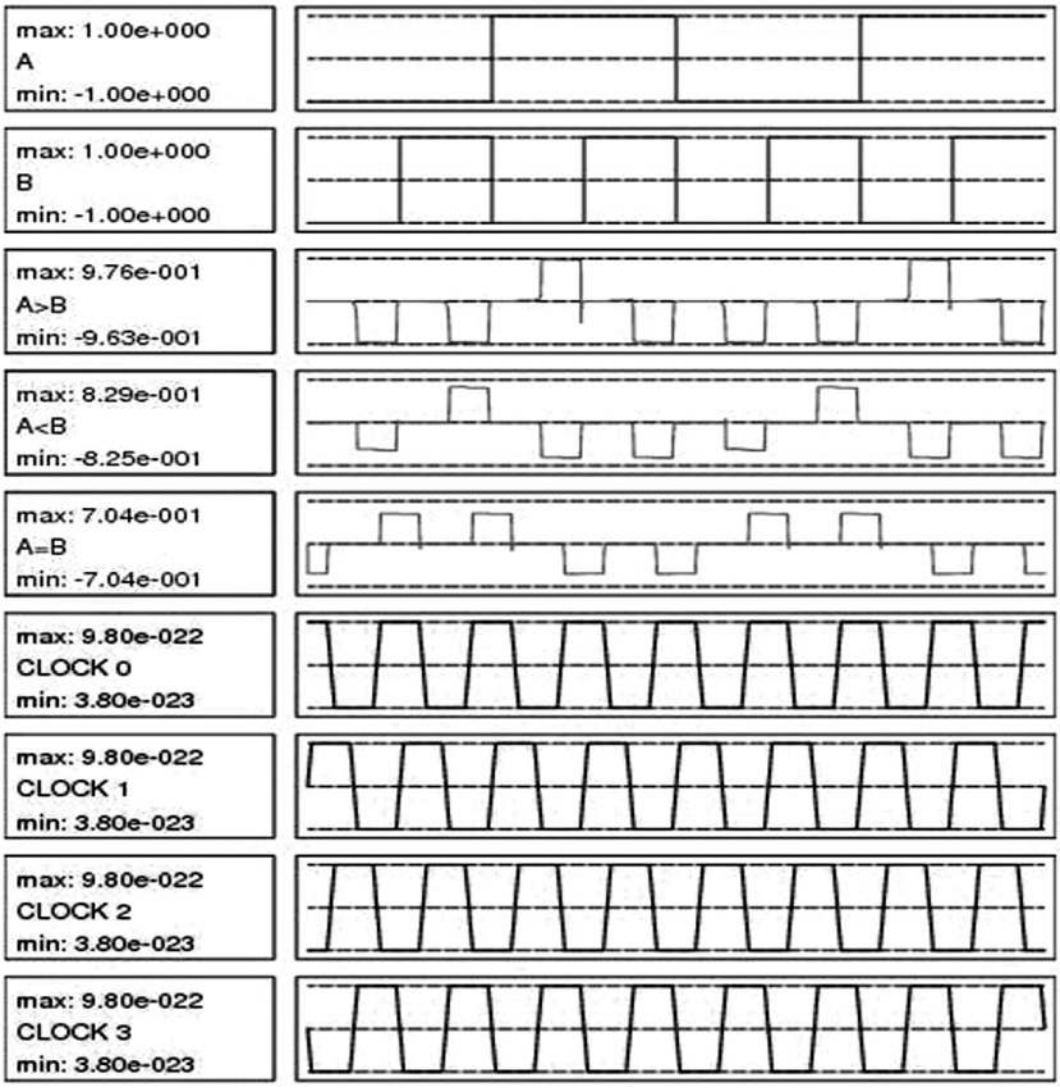

FIGURE 6.13 Simulation result of proposed single-bit reversible comparator.

6.5 LOGIC-LEVEL IMPLEMENTATION

The comparator is implemented using Verilog hardware description language (HDL) on Xilinx ISE 13.1 platform. First the Verilog modules of

reversible gates, namely Feynman and Fredkin are developed. Further, these modules are instantiated to form a top-level module shown in Figure 6.11. The synthesis result is shown in Figure 6.14. It has two inputs A and B, five outputs AgtB (A greater than B), AltB (A less than B), and AeqB (A is equal to B) along with two GOs (gar 1and gar 2).

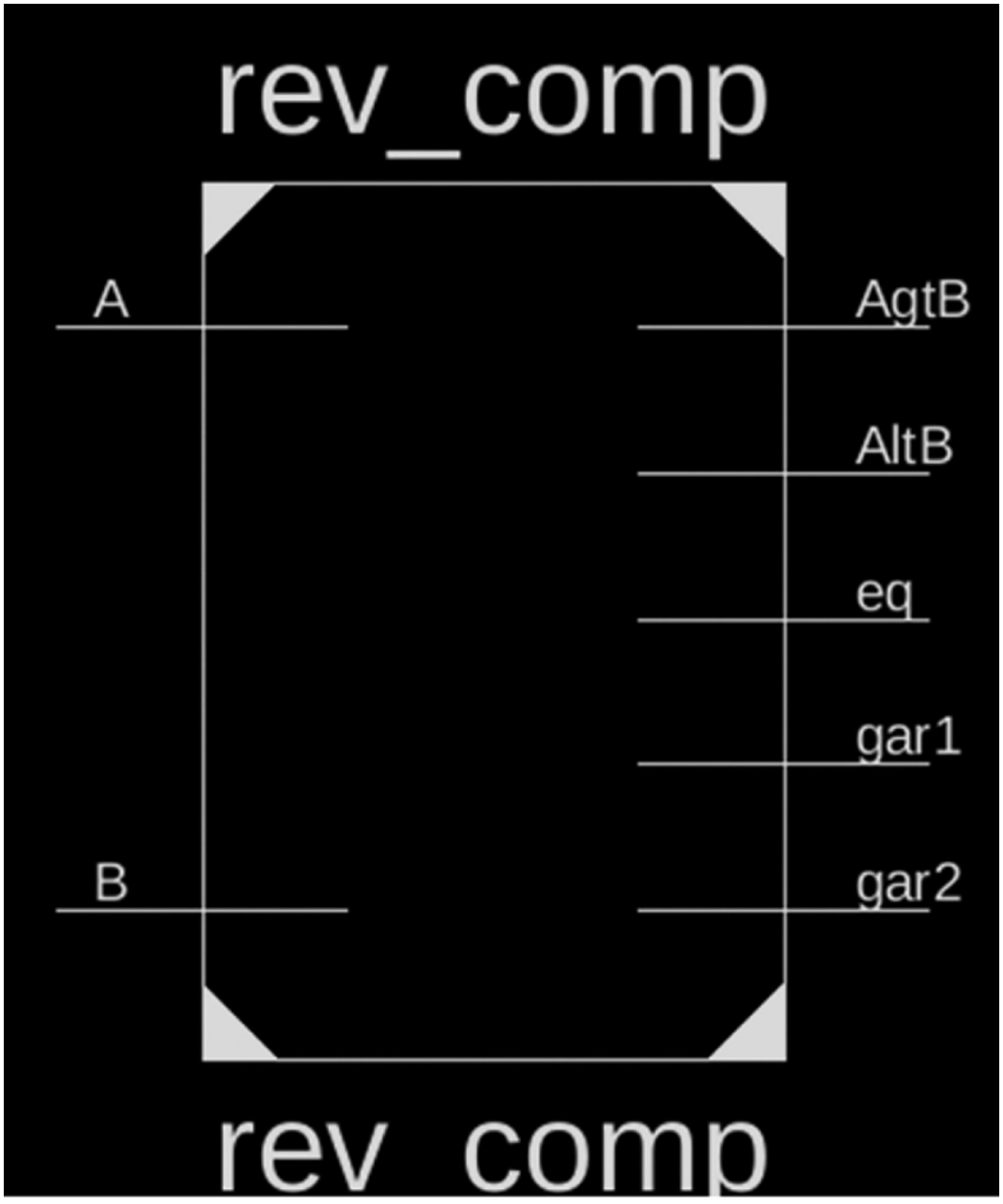

FIGURE 6.14 RTL schematic of proposed comparator.

The logic-level schematic of the comparator is shown in Figure 6.15. It is seen from Figure 6.15 that it consists of reversible gates, namely Feynman and Fredkin to form the proposed comparator as shown in Figure 6.11.

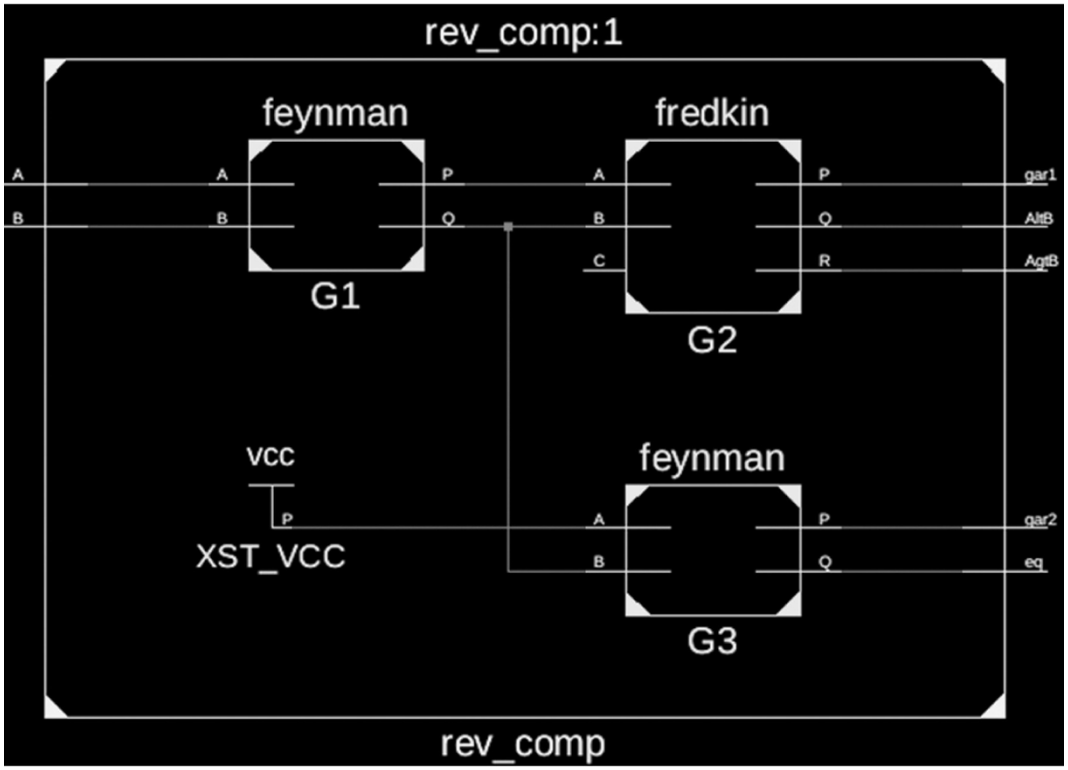

FIGURE 6.15 Logic-level implementation of proposed comparator.

The behavioral simulation is carried out and shown in Figure 6.16. The outputs AgtB (A greater than B), AltB (A less than B), and AeqB (A is equal to B) for respective inputs are highlighted in Figure 6.16. It is observed that the output for the proposed comparator is obtained properly at the logic level.

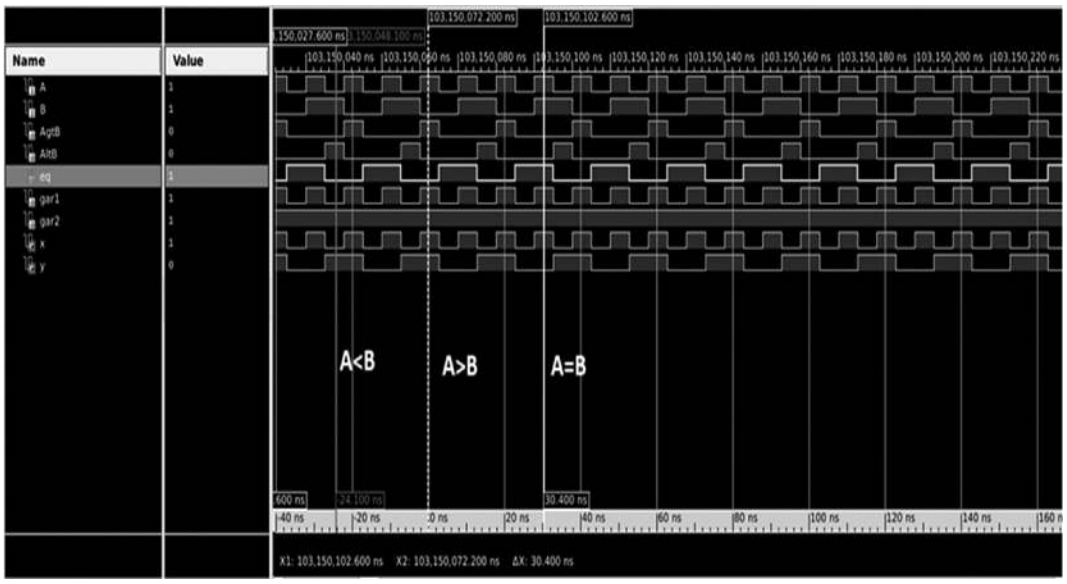

FIGURE 6.16 Simulation result of proposed comparator.

6.6 DEFECT ANALYSIS

QCA being at the nanoscale, the occurrence of defects is obvious in it. The complete defect analysis was carried out in Ref. [11]. The defects are classified into two categories, namely synthesis phase and deposition phase. In the synthesis phase, the cell is fabricated and deposited on the silicon substrate in the deposition phase. The deposition phase defects are cell misalignment, displacement, single missing cells, and multiple missing cells. The multiple missing cell defect model for QCA is proposed in Ref. [12]. Displacement defects with analytical methods are proposed in Ref. [13]. In this chapter, a single missing cell defect is considered. The main primitive of QCA is MV. So, in this section, the first single missing cell defect analysis for MV is discussed followed by the proposed comparator's defect. The single cell of MV as shown in Figure 6.3 is removed one by one and the simulation is carried out using the QCADesigner-E tool. Same simulation parameters mentioned in Table 6.1 are used. The simulation result for input A missing cell is shown in Figure 6.17. The results for

single missing cell defect analysis carried out for MV are summarized in Table 6.2.

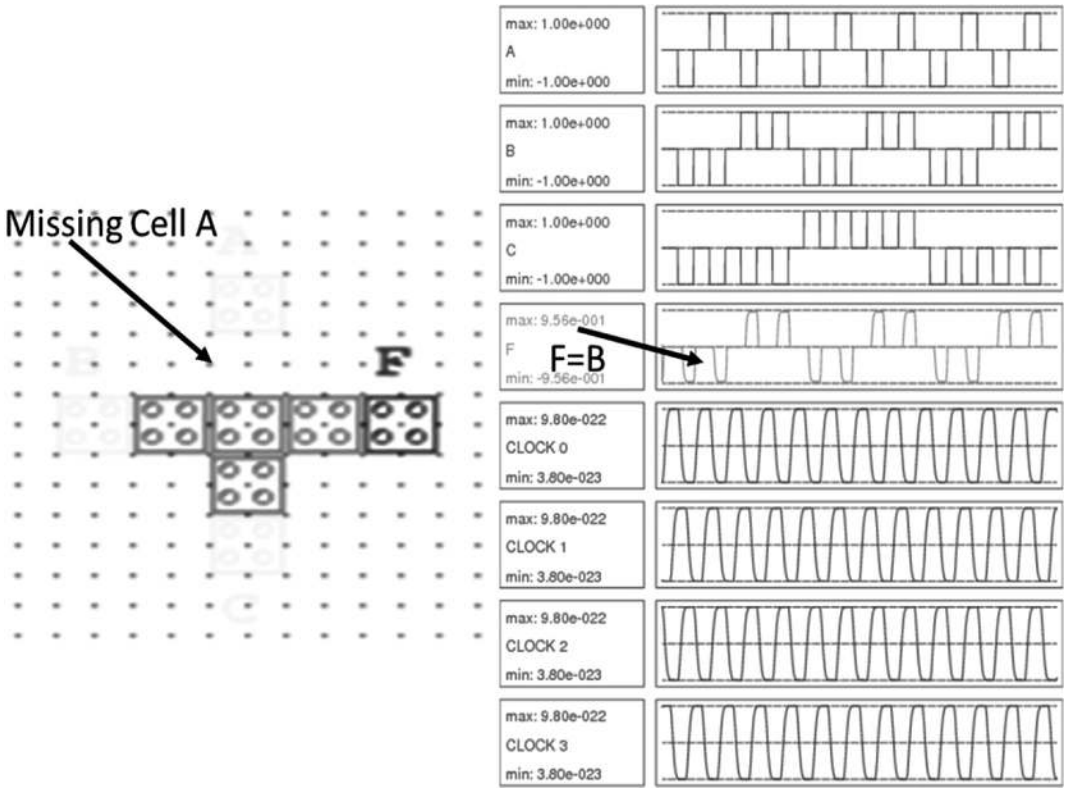

FIGURE 6.17 Single missing cell defect in majority voter.

TABLE 6.2 Single Missing Cell Analysis of Majority Voter.

Sr. No.	Missing Cell	Output	Faults
1.	A	B	S-a-B
2.	B	B	–
3.	C	B	S-a-B
4.	D	M (A’ B C’)	M (A’ B C’)
5.	F	Low polarization	–

When input cell A is missing, the output F is the same as input B. Similarly, the output is the same as the input B when input cell C is missing.

No effect on output is observed when cell B is missing while the missing of middle cell D causes the output function M (A’ B C’). When the output cell itself is missing then low polarization is obtained.

The single missing cell defects in MV at the device level cause two types of faults at the logic level, namely output is permanently stuck at input B, that is, S-a-B fault and output F = A'B+BC'+A'C', that is, M (A'B C'). These two faults as a consequence of single missing cell defects in MV are mentioned in the last column of Table 6.2.

Single missing cell analysis for sequential reversible circuits is presented in Ref. [14]. Recently, authors have presented a reversible comparator's defect analysis in Ref. [15].

Further, in this chapter, the single missing cell analysis carried out for MV is applied to the reversible Feynman and Fredkin gates. The consequences of these effects are then analyzed for the proposed comparator. For this purpose, an extensive simulation of the proposed design is carried out. The effect of single missing cell defects in MV: reversible gates on the comparator output A > B, A < B, and A = B are summarized in Table 6.3.

TABLE 6.3 Single Missing Cell Analysis of the Proposed Comparator.

Feynman Gate 1				
Faults	**Output**		**Comparator Output**	
	Q = A'B+AB'	**A < B A'B**	**A > B AB'**	**A = B AB+A'B'**
MV1 at S-a-B	AB'	0	AB	AB'+A'
MV1 at M (A' B C')	AB'	0	AB	AB'+A'
MV2 at S-a-B	A+A'B	A'B No change	AB' No change	A+A'B'
MV2 at M (A' B C')	AB+A'B	A'B No change	AB' No change	AB+AB'
MV3 at S-a-B	1	A'	0	A
MV3 at M (A' B C')	AB+A'B'	A'B'	0	AB

The Feynman gate shown in Figure 6.8 consists of three MV, namely MV1, MV2, and MV3. The single missing cell effects in each MV are summarized in Table 6.3. This Feynman gate is one of the blocks of the comparator shown in Fig. 6.11. The consequences of Feynman defects on the comparator output A < B, A > B, and A = B are mentioned in Table 6.3. It is observed that the single missing cell defects of the Feynman gate are affecting the output A = B more comparator to the outputs A < B and A > B.

6.7 COMPARATIVE ANALYSIS

Energy dissipation is one of the important parameters in the reversible circuit. The QCADesigner version E has an inbuilt feature to calculate the energy of a QCA circuit. The average energy dissipation of the proposed comparator for device-level implementation is 1.16e-002 eV. Table 6.4

represents the comparison of the proposed design with the already available design discussed in this chapter [16].

TABLE 6.4 Parameters Analysis of Proposed Design.

Sr. No.	Performance Parameter	Proposed Work	XOR-Based Design Implemented in This Chapter [16]
1.	Quantum cost	7	5
2.	Garbage output	2	1
3.	Average energy dissipation	1.16e–002 eV	1
4.	Remarks	All three outputs	It doesn't have the output signal for equals to.
5.	Defect analysis	√	–

In this chapter, the logic-level implementation using Verilog HDL is also carried out which is missing in almost all available literature for reversible comparator. This implementation is useful to observe the hardware behavior of the proposed design on FPGA. In addition, the single missing cell defect analysis is carried out using QCADesigner's extensive simulation at the device level to show the fault tolerance of the proposed comparator. This analysis is not available in Ref. [16].

6.8 CONCLUSION

The proposed reversible technology-based comparator consisting of Fredkin and Feynman reversible gates is implemented at the device level using QCA nanotechnology. The proposed design has 1.16e-002 eV energy dissipation and a QC of 7. The logic-level implementation is also proposed using Verilog HDL through the Xilinx ISE platform to verify and compare the results with the device level. This logic-level implementation can be used for the field programmable gate array (FPGA). Further, the single missing cell defect analysis of the proposed comparator is carried out to show the fault tolerance of it.

6.9 FUTURE WORK

The defect analysis for displacement, misalignment, and multiple missing cell analysis can be carried out. Also, the FPGA implementation to observe the behavior of the proposed design in hardware can be carried out.

KEYWORDS

- **comparator**
- **Fredkin gate**
- **Feynman gate**
- **garbage output**
- **majority voter**
- **quantum-dot cellular automata**
- **quantum cost**

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CHAPTER 7

Investigation of Optoelectronic Characteristics of Double Quantum Well Structure for Triangular Well Geometry

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ABSTRACT

The present chapter deals with computation of absorption coefficient and oscillator strength for triangular double quantum well triple barrier structure for optical photodetector applications. For different structural, material, and characteristic parameter modifications, the lowest intersubband energy for a double quantum well structure is computed using the triangle potential. When compared to DQW structures, the finding is significant since the peaks of the transmission coefficient characteristic curve lack a quasi-peak, suggesting very minimal energy band spreading. The results have consequences for the design of MWIR photodetectors. For a variety of

internal and structural parameters, the absorption coefficient of a double quantum well structure is also computed for the triangle potential in the presence of an electric field. Customizing the design limitations within the manufacturing limit optimizes the absorption profile. It is evident that the current configuration is more appropriate for high frequency applications when the outcome is contrasted with rectangular shape.

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7.1 INTRODUCTION

Electronic components made with nanoscale materials and construction methods are known as nanoelectronic devices. In comparison to conventional electronic devices, nanoelectronic devices can offer faster speed, higher density, lower power consumption, and superior reliability [1]. They can also increase the performance and efficiency of current technology. They can also make new features and functions conceivable that are not achievable with the technology available now. New applications and advancements in a variety of sectors are made possible by nanoelectronic devices. They may present fresh avenues for investigation and growth in fields including information technology, green energy, nanomedicine, and more. New markets and industries that are beneficial to society and the economy can also be produced by them. The study of physical and quantum events that take place at the nanoscale can be facilitated by nanoelectronic devices [2, 3, 4, 5, 6, 7, 8, 9 and 10], which can contribute to the advancement of fundamental knowledge in physics and chemistry. Additionally, they can aid in the discovery of novel materials and their properties.

In addition, other kinds of structures like quantum wires and quantum dots can also experience quantum confinement. The electrical characteristics of quantum wires, which are long, thin structures in one dimension, are comparable to those of quantum wells. Conversely, tiny, three-dimensional structures known as quantum dots are present. In this scenario, the energy levels become extremely discrete, and by adjusting the quantum dot's size and shape [11], the material's electrical characteristics can be controlled.

Experimental methods for observing the effects of quantum confinement include photoluminescence, absorption spectroscopy, and tunneling spectroscopy. By measuring the confined particles' optical and electrical characteristics, these methods provide light on the system's quantum behavior. In conclusion, a fundamental phenomenon known as quantum confinement happens when a particle is held in a space that is smaller than its de Broglie wavelength. The particle's energy levels become quantized as a result of this confinement, which has important ramifications for the material's optical and electrical characteristics. Because quantum confinement has so many potential applications, it is extensively studied in photonics, electronics, and nanotechnology.

The Schrödinger equation, which addresses the potential energy brought on by the electrons' trapping inside the well, can be used to characterize the electronic characteristics of a quantum well [12, 13, 14 and 15]. A discrete set of permitted energy levels quantizes the electrons' energy levels in the well. Because of the electrons' confinement, these energy levels are more closely spaced than those in an unconfined material. The quantization of the electronic energy levels results in unique optical characteristics for a quantum well. The well's absorption of light facilitates the excitation of electrons from the uppermost quantum state of valence band to the

lowermost quantum state of conduction band, which causes the electrons to recombine and release light [16]. The energy spacing between the electronic energy levels in the well, which can be adjusted by changing the well's thickness or the materials it is made of, determines the energy of the light that is released.

7.2 EIGENSTATES AND INTERSUBBAND TRANSITION IN A QUANTUM WELL

Understanding the behavior of quantum systems requires the computation and interpretation of eigenstates, a key idea in quantum mechanics. An eigenstate is a situation where a particular observable is in a fixed state within the system. For example, when measuring a particle's position, it may be in several places at once, but we can pinpoint its precise location when taking the measurement. An eigenstate is the state in which it occupies a specific location. Stated differently, eigenstates are those conditions in which the system's characteristics are clearly defined.

Eigenstates have several implications, one of which is that they help us comprehend a system's energy levels. The set of eigenstates for a system represents all the potential energy levels that the system may have. Each eigenstate is linked to a particular energy. These data can be used to forecast the results of energy measurements, like those made in spectroscopy experiments. We can comprehend a system's behavior and characteristics by knowing its eigenstates. Eigenstates also have the significant consequence of helping us comprehend how a system changes over time. A superposition of a quantum system's eigenstates, each of which evolves with a distinct phase factor, can be used to depict the time evolution of the system. This means that the behavior of a system can be understood by considering the amplitude and phase of each eigenstate. By knowing the

eigenstates of a system, we can predict how it will evolve over time and make accurate predictions about future measurements.

7.3 ABSORPTION COEFFICIENT FOR QUANTUM WELL

The rate at which light is absorbed by the well's electrons as it travels through the material is indicated by the absorption coefficient and oscillator strength for a quantum well. The energy and polarization of the incident light, as well as the thickness and material composition of the quantum well, all affect the absorption coefficient. Fermi's golden rule, which links the square of the perturbation matrix element driving the transition to the transition rate between two quantum states, can be used to calculate it [17]. The interaction of the electrons with the incident light is the perturbation for a quantum well. In a quantum well, absorption is the process by which an electron in the well absorbs a photon of a particular energy, resulting the electron to transit toward higher quantum level. When the photon's energy equals the difference in energy between two quantum well energy levels, absorption takes place.

Because of the electrons' confinement inside the well, the electronic states in a quantum well are quantized. There are energy gaps between the discrete permitted electronic energy levels in the well. The electron can absorb the photon and move from the lower energy level to the higher energy level when it is incident on the well with energy equal to the energy gap between two levels. The Fermi–Dirac distribution function, which expresses the likelihood of an electron occupying a specific energy level, the density of states within the well, and the strength of the electron–photon interaction all influence the probability of photon absorption in a quantum well. Infrared detectors and quantum cascade lasers, which depend on the effective absorption and emission of photons to achieve their intended functionality, are two examples of applications of absorption in quantum

wells. Controlling the absorption coefficient and customizing the device for a given application is possible by manipulating the quantum well's properties.

7.4 IMPORTANCE OF TRIANGULAR QUANTUM WELL

The energy of a particle in a potential well is represented mathematically by the triangular potential. Its definition is given by the potential strength parameter and a hyperbolic cosine function. The inner region and the outer region are the two regions that make up the potential well. The particle can move freely in the inner region, where the potential is negative. In contrast, the particle is trapped in the well in the outer region where the potential is positive. It is a one-dimensional potential made up of two superposed hyperbolic cosine functions. When the triangular potential is inverted around the *x*-axis, it assumes the same shape, which is known as symmetry. Whether the particle is on the left or right side of the well, the system's energy remains constant because the potential is symmetric about the well's center. This symmetry is crucial because it frees us from having to take into account the behavior of each individual particle and instead enables us to predict the system's behavior based on its overall shape and structure. This facilitates the modeling of complex systems and the prediction of their behavior in various scenarios.

The triangular potential only allows a subset of energy levels for the quantum mechanical system due to its discrete spectrum. This property is similar to the limited behavior of atoms' electrons at specific energy levels. The potential's analytical solution to the Schrödinger equation allows for the computation of wavefunctions and energy levels for a particle in the potential. Unlike some other potential models, the triangular potential can be described by a relatively simple mathematical formula. This makes it

easier to compute and run simulations, and it lets scientists use mathematical models to predict how real-world systems will behave.

There are numerous uses for the triangular potential in quantum mechanics. Its primary use is in the analysis of molecular and atomic spectra. The Schrödinger equation, a key formula in quantum mechanics, can be used to determine the energy levels of atoms and molecules. The Schrödinger equation for a given system can be solved using the triangular potential, and the energy levels that are produced can be used to forecast the system's spectral lines. The characteristics of quantum dots [18], which are minuscule semiconductor particles with distinct optical and electronic properties, are also studied using the triangular potential [19].

In molecular spectroscopy, the triangular potential is frequently utilized to simulate how electromagnetic radiation interacts with molecules. The potential's capacity to precisely characterize the behavior of molecules in both their excited and ground states gives rise to this application. In semiconductor physics, the triangular potential is also employed to simulate the energy band structure of semiconductors. Potential information can shed light on semiconductors' electrical characteristics, including the bandgap and electron energy levels. The triangular potential is a useful tool for theoretical calculations because it can be used as an approximation for more complex potentials [20]. Overall, because of its analytical solvability, mathematical simplicity, and broad applicability, the triangular potential is a significant and extensively researched potential function in quantum mechanics.

7.5 LITERATURE REVIEW

As compared with previous works on rectangular profile [21, 22 and 23], parabolic [24, 25, 26, 27 and 28], and Gaussian [29, 30 and 31], Pösch-Teller [32, 33, 34 and 35] are the potential geometries that are being

researched the most because of their utility in predicting the electrical and optical properties of low-dimension devices. Since complex potentials are difficult to solve using analytical techniques, various numerical techniques are also taken into consideration for an accurate calculation. Due to their accuracy, the finite element method [36, 37] and the finite difference method [38, 39] are the most widely used among the various techniques; however, these methods have drawbacks in terms of computation time and memory usage. Although it takes the least amount of time, the transfer matrix technique is only applicable to rectangular structures [40]. Because it takes less time to estimate as an intermediate solution, the propagation matrix method [41] attracts workers' attention.

In order to solve the triangular potential with extremely little error for the design of a photodetector at MWIR-LWIR bands, Ricardo et al. [42] used the transfer matrix method. The potential is subjected to a later canonical transformation method [43]. Triangular and other hypergeometric potentials were solved using the Klein–Gordon equation by Ikot and colleagues [44], yielding bound state solutions. For the purpose of determining the wavefunction, the Nikiforov–Uvarov method is also attempted [45]. Later, generated scatterings are interpreted [46] for device applications. A pure mathematical variation of the concept of position-dependent effective mass was introduced relatively recently [47]. To the best of the authors' knowledge, however, relatively little research has been done on the optical characteristics of quantum structures based on triangular potential to date.

7.6 OBJECTIVE OF THE PRESENT WORK

The current work uses the propagation matrix technique to compute the eigenstates of a double quantum well structure using the triangular potential. Eigenstates of double quantum well structure using triangular potential are computed by the propagation matrix technique.

Positiondependent effective mass is considered following BenDaniel Duke condition, and conduction band nonparabolicity is assumed. Field is applied within practical limit, and transmission characteristics are investigated based on resonant tunneling phenomenon. Results are compared with the already published literatures. The field is used as far as it is practicable, and the resonant tunneling phenomenon is used to study the transmission characteristics. The results are contrasted with rectangular profiles and previously published literature. The simulated result has profound physical implications for the design of quantum detectors in the midwave infrared.

7.7 MATHEMATICAL FORMULATION FOR ELECTRONIC AND OPTOELECTRONIC PROPERTIES

Schrödinger's time-independent equation may be used to calculate the motion of a single electron in one dimension when an external electric field is present. The fundamental equation is represented in the following manner:

$$-\frac{\hbar^2}{2}\frac{\partial}{\partial y}\left[\frac{1}{m^*(y)}\frac{\partial}{\partial y}\psi(y)\right]+V(y)\psi(y)-q\xi(y)y=E(y)\psi(y) \qquad (7.1)$$

where we have considered the effective mass mismatch, ζ (*y*) is the electric field along the y-direction. The solution of Schrödinger's Equation (7.2) necessitates an envelope function approximation that is both (1/m^*) (∂φ (*y*)/∂*y*) and φ (*y*) are continuous by taking electron transport across the heterojunction to prevent differentiating discontinuous functions and creating infinities.

In the barrier and well regions as defined in Equation (7.1), the modified form of Schrödinger's equation may be put as

$$-\frac{\hbar^2}{2}\frac{\partial}{\partial y}\left[\frac{1}{m_b^*(y)}\frac{\partial}{\partial y}\psi(y)\right]+V_b(y)\psi(y)-q\xi(y)y=E(y)\psi(y) \tag{7.2}$$

and

$$-\frac{\hbar^2}{2}\frac{\partial}{\partial y}\left[\frac{1}{m_w^*(y)}\frac{\partial}{\partial y}\psi(y)\right]+V_w(y)\psi(y)-q\xi(y)y=E(y)\psi(y) \tag{7.3}$$

where m_{w}^* and m_{b}^* are the effective masses of well and barrier regions, respectively, following Equation (7.3) and Equation (7.2), and V_{w} and V_{b} are potentials respectively for the same. Wavevector for the present problem may be defined as:

$$k_j=\left[\frac{2m^*(E-qV_j)}{\hbar^2}\right]^{0.5} \tag{7.4}$$

where the term V_{j} stands for potential function, which includes both $V_{\mathrm{b/w}}$ and field component along the propagation direction.

The wave functions as computed from the Schrodinger equation in regions "*j*" and "(*j* + *1*)" are

$$\psi_j=A_j\exp[ik_jy]+B_j\exp[-ik_jy] \tag{7.5}$$

$$\psi_{j+1}=C_{j+1}\exp[ik_{j+1}y]+d_j\exp[-ik_{j+1}y] \tag{7.6}$$

where *B* and *D* are the equivalent right-to-left traveling-wave coefficients, while *A* and *C* are coefficients for the wave function traveling left to right in regions *j* and *j* + 1, respectively. It is assumed that every connection satisfies the boundary requirements set out by Ben Daniel Duke.

Propagation between potential steps separated by distance L_{j} carries phase information only so that

$$\psi A_j\exp[ik_jL_j]=\psi C_j \tag{7.7}$$

sand

$$\psi B_j \exp[-ik_j L_j] = \psi D_j \tag{7.8}$$

This can be formulated as

$$\begin{bmatrix} A_j \\ B_j \end{bmatrix} = M \begin{bmatrix} C_{j+1} \\ D_{j+1} \end{bmatrix} \tag{7.9}$$

where

$$M = \begin{bmatrix} \exp[-ik_j L_j] & 0 \\ 0 & \exp[ik_j L_j] \end{bmatrix} \tag{7.10}$$

As a result, the propagation matrix for the *j*th area is expressed as

$$P_j = \frac{1}{2} \begin{bmatrix} \left(1 + \frac{m_j}{m_{j+1}} \frac{k_{j+1}}{k_j}\right) \exp[-ik_j L_j] & \left(1 - \frac{m_j}{m_{j+1}} \frac{k_{j+1}}{k_j}\right) \exp[-ik_j L_j] \\ \left(1 - \frac{m_j}{m_{j+1}} \frac{k_{j+1}}{k_j}\right) \exp[ik_j L_j] & \left(1 + \frac{m_j}{m_{j+1}} \frac{k_{j+1}}{k_j}\right) \exp[ik_j L_j] \end{bmatrix} \tag{7.11}$$

The transmission matrix is provided by a flow of propagation matrix in various regions of the involved structure, and it is defined as

$$T(E) = \frac{1}{(P_{11})^2} \tag{7.12}$$

Optical absorption coefficient for arbitrary quantum well device can be written in the following form:

(7.13)

$$\alpha(\omega) = \frac{q^2 m^*}{2\varepsilon_0 \varepsilon_r c n_r \hbar d m_0^2} \frac{M^2}{\hbar\omega} \times \sum\nolimits_{n,m} \langle \xi_v^m \mid \xi_c^n \rangle \Theta(E_{mn} - \hbar\omega)$$

where $\langle \xi_v^m \mid \xi_c^n \rangle$ is the integral function that denotes the overlap between the envelope functions of valence and conduction bands respectively, "*d*" denotes the quantum well width, Θ represents Heaviside step function, and "*M*" is defined as

$$M = N \int_{\text{cell}} \psi_{\kappa_e}^* \left(\overrightarrow{r'}\right) p_A \psi_{\kappa_v} \left(\overrightarrow{r'}\right) dv \tag{7.14}$$

In Equation (7.13), the integral function gives the selection rule between two adjacent quantum states. It may be written in the form:

$$\langle \xi_v^m \mid \xi_c^n \rangle = \delta_{\mathrm{K,K'}} \int_{-d/2}^{d/2} \chi_m^h(Z) \chi_n^e(z) dz \tag{7.15}$$

where it may be noted that we have considered *z*-axis as the direction of applied field. Here, the wave functions χ_{i} is selected from the generalized solution of the Schrödinger wave equation.

Substituting the values of wave functions with some rearrangement, we get

$$\alpha(\omega) = \frac{2\pi q^2 \hbar}{\varepsilon_0 \varepsilon_r c n_r m^{*2} V} \frac{1}{\hbar\omega} \times \left\langle \sum_{i,j} |\langle i|p_z|j\rangle|^2 \mid \delta(E_j - E_i - \hbar\omega)\left(f_{FD}{}^i - f_{FD}{}^j\right) \right. \tag{7.16}$$

where "*i*" and "*j*" are the initial and final states, and f_{FD} is the Fermi–Dirac distribution function. Kronecker delta function is introduced to conserve the momentum.

Introducing Lorentzian line shape function and the concept of oscillator strength, we get

$$\alpha(\omega) = \frac{n_s \pi q^2 \hbar}{\varepsilon_0 \varepsilon_r c n_r m^{*2} d} \frac{1}{\hbar\omega} \left[\frac{8\hbar}{3d}\right]^2 \delta(\Delta E - \hbar\omega) \tag{7.17}$$

Define oscillator strength between the first and second states as

$$f_{21} = \frac{2}{\hbar m \omega} \left[\frac{8\hbar}{3L}\right]^2 \tag{7.18}$$

Fermi's golden rule is a formula that describes the transition rate (the probability of a transition per unit time) from one energy eigenstate of a quantum system to another energy eigenstate, as a result of a weak perturbation. The general form of Fermi's golden rule is

$$R_{i\to f} = \frac{2\pi}{\hbar} \left| \left\langle f \middle| V \middle| ^2 i \rho(E_f) \right. \right. \tag{7.19}$$

where $R_{i\to f}$ is the transition rate from initial state $|\, i \,\rangle$ to final state $|\, f \,\rangle$, V is the perturbation operator, $\rho(Ef)$ is the density of states at the final energy E_f, and $\hbar$ is the reduced Planck's constant. To apply Fermi's golden rule to intersubband transitions, we need to specify the perturbation operator and the density of states for the quantum well system.

The density of states for a quantum well system depends on whether we consider electrons or holes, and whether we consider triangular or nontriangular subbands. We will assume for the sake of simplicity that the

electrons in question are in triangle subbands. The density of states in this instance is provided by

$$\rho(E) = \frac{m^*}{\pi\hbar^2} \tag{7.20}$$

where *m* * is the effective mass of the electron.

Using these expressions, we can write Fermi's golden rule for intersubband transitions as

$$R_{i\to f} = \frac{2\pi}{\hbar}\left|e\left\langle f\right|r.E\left|i\right\rangle\right|^2\frac{m^*}{\pi\hbar^2} \tag{7.21}$$

This formula gives us the probability per unit time that an electron in subband | *i* ⟩ will make a transition to subband | *f* ⟩ due to the absorption of a photon with electric field *E*. Note that this formula assumes that there are no other processes that affect the transition rate, such as scattering or relaxation.

The oscillator strength in the calculated absorption cross section can be obtained as

$$\sigma_{2,1} = \frac{q^2T}{2\varepsilon_0 m^* nc} f_{21}\left[1+T^2\left(\frac{E-\Delta E_{2,1}}{\hbar}\right)^2\right]^{-1} \tag{7.22}$$

where "*T*" is the relaxation time.

7.8 RESULTS AND DISCUSSIONS

Based on the mathematical formulation discussed in the previous section, electronic properties of the structure under consideration are computed and plotted. Results can be subdivided into two sections: the first calculation is carried out in the absence of electric field, and next by applying the field.

Figure 7.1 shows the biasing effect on triangular configuration. It is found that with increase of applied bias, energy peaks appear at lower values, which is quite expected owing to reduction of quantum confinement. But the interesting feature noted in this case is the nonexistence of quasi-peak even at higher Eigen states, which exist in a rectangular profile.

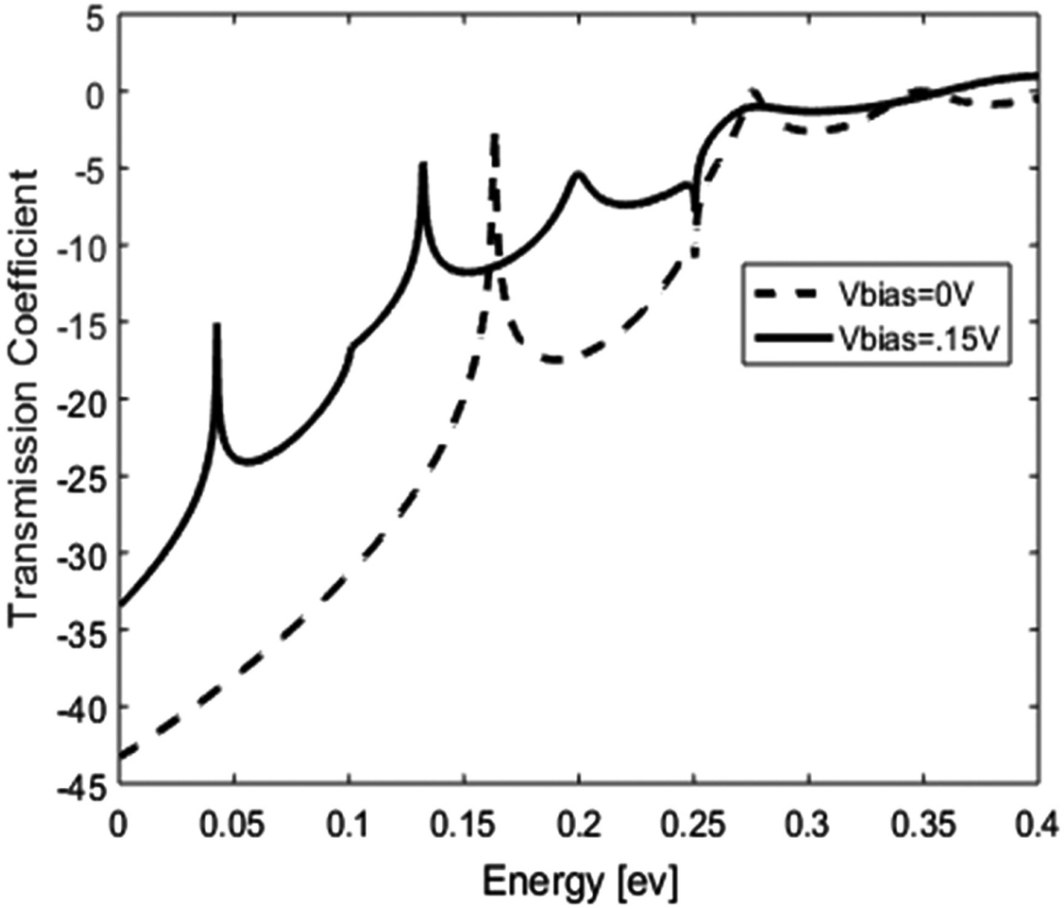

FIGURE 7.1 Transmission coefficient as a function of energy in the presence and absence of bias.

Effect of varying dimensions is computed and plotted in Figure 7.2. Dimensions are considered within fabrication limit, and well width, contact barrier width, as well as middle barrier width is modified to observe the change in magnitude and positions of eigen-peaks. Figure 7.2a shows that

for varying well width, the position of lowermost eigenstate remains unchanged, whereas higher energy states make a redshift. This is evident in Figure 7.2a, which speaks in favor of tuning the intersubband transition.

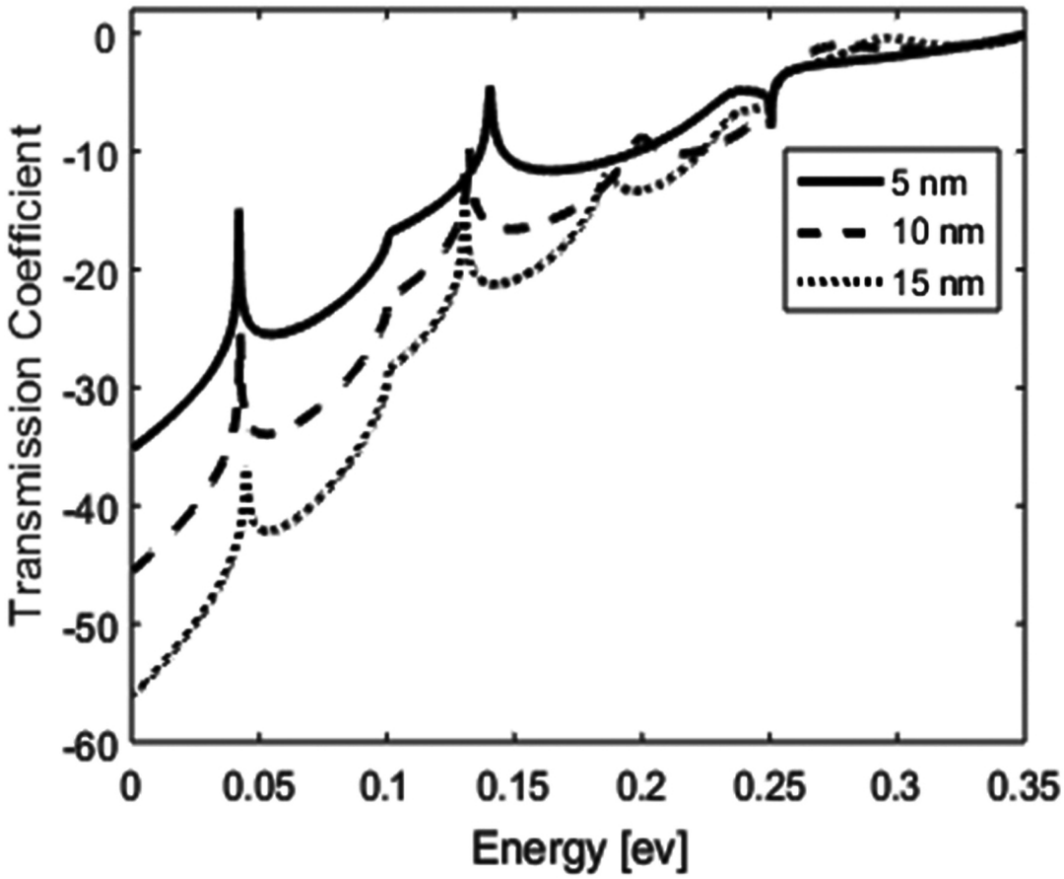

FIGURE 7.2a Transmission coefficient as a function of energy for three different well widths in the presence of bias.

From Figure 7.2b, it is observed that the magnitude of intersubband transition remains almost independent of contact barrier dimensions, whereas middle barrier width can greatly influence it. This is plotted in Figure 7.2c. A larger middle barrier width increases the subband energy, which speaks for photodetector operating at a lower wavelength region.

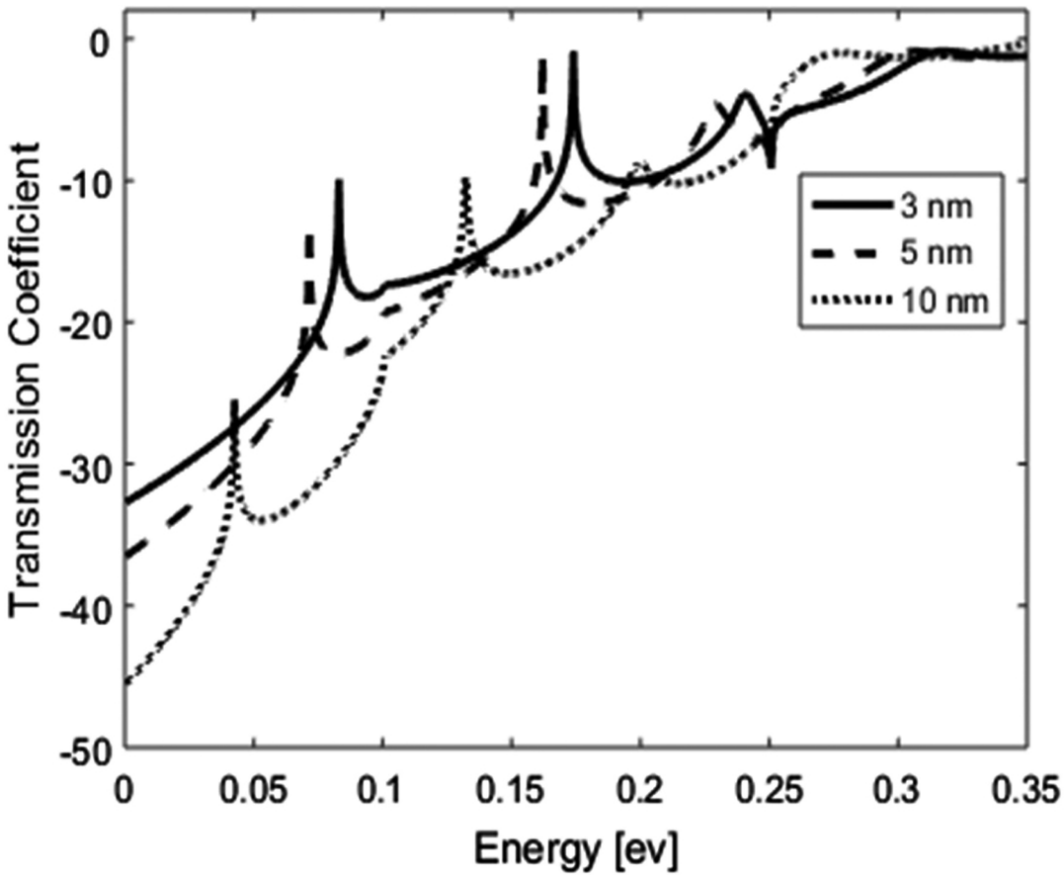

FIGURE 7.2b Transmission coefficient as a function of energy for three different contact barrier widths in the presence of bias.

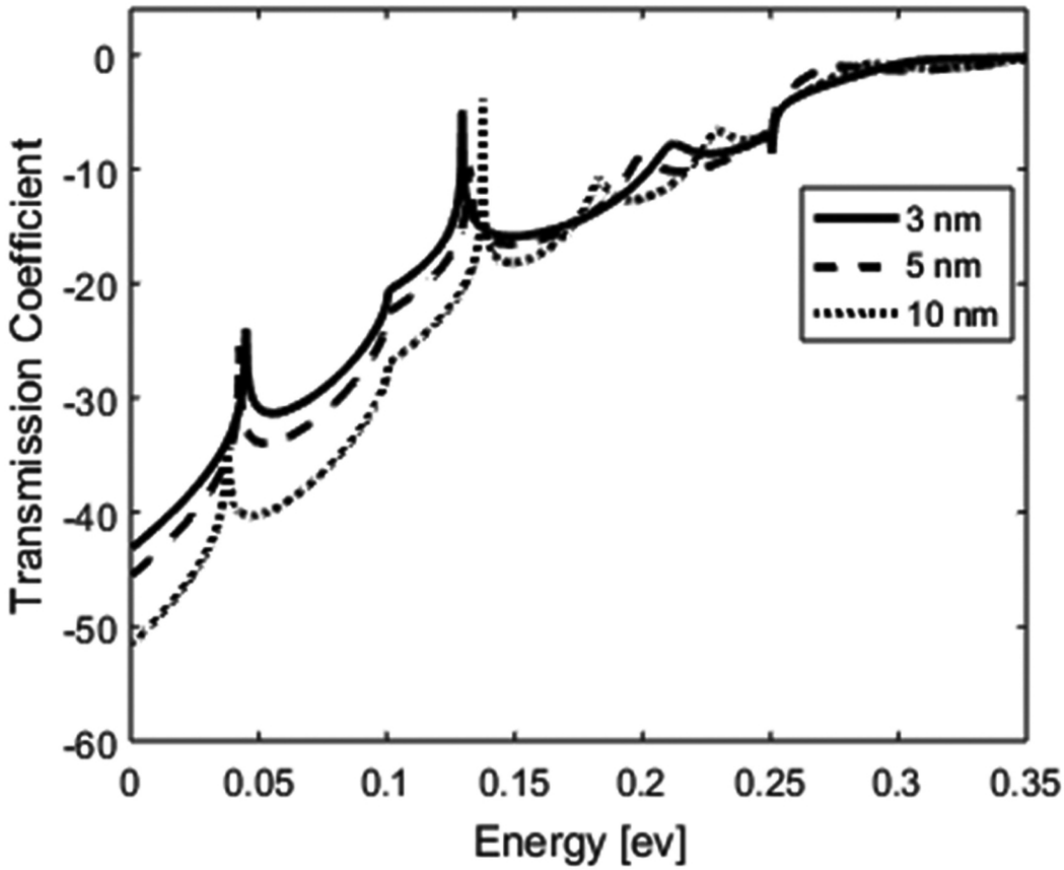

FIGURE 7.2c Transmission coefficient as a function of energy for three different middle barrier widths in the presence of bias.

Figure 7.3 shows the variations for different material compositions. Lowering the Al content in barrier material reduces the quantum confinement which, in turn, decreases the potential barrier. But the intraband energy remains almost constant. The result is also plotted for type-II system, where $x = 0.5$ is considered. In this context, it may be mentioned that we have considered symmetric DQW structure, that is, barrier material composition in all the layers is exactly the same.

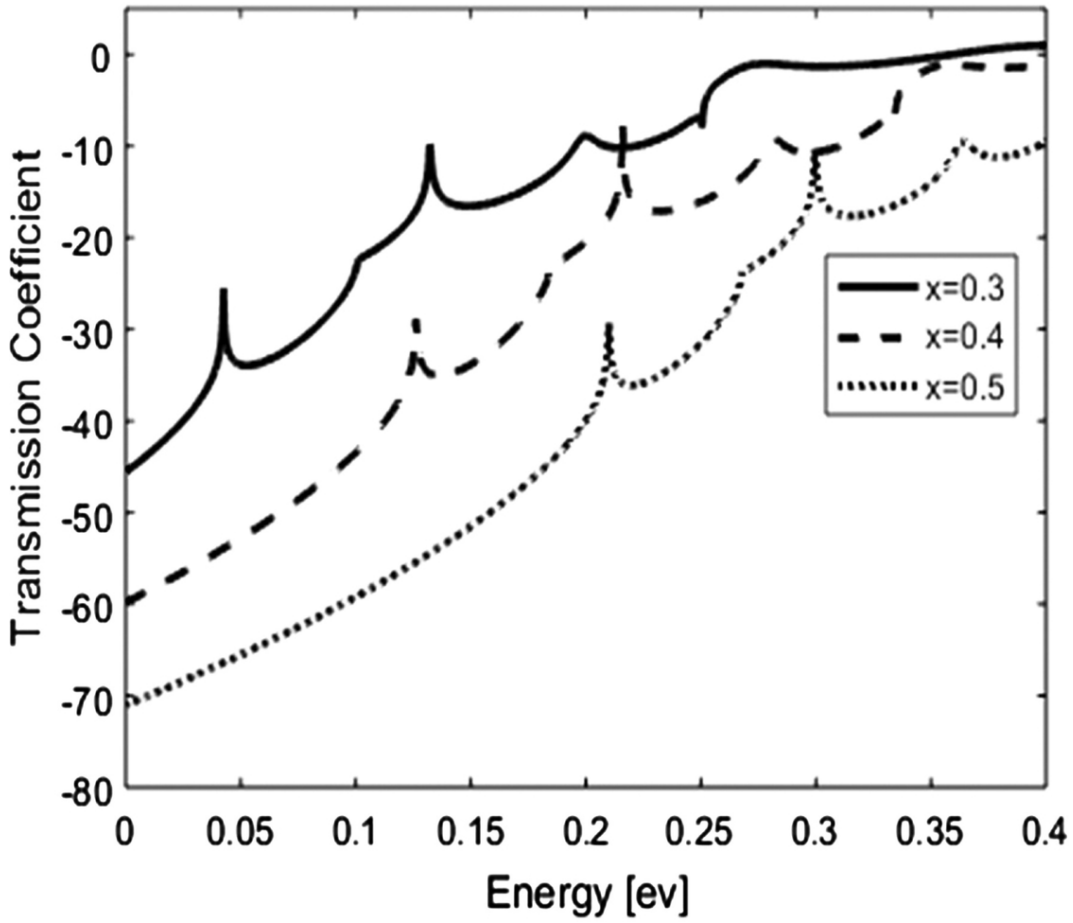

FIGURE 7.3 Transmission coefficient as a function of energy for three different material compositions in the presence of bias.

Now, to test the quality of the photodetector we compute the absorption coefficient and oscillator strength dependence on intersubband transition in the quantum well. The layer dimensions and material compositions are kept constant, and the absorption coefficient and oscillator strength are computed and plotted for first three intersubband transitions considering the first three eigenstates.

Figure 7.4 shows the variation of absorption coefficient with wave-length for the structure under consideration. Figure 7.4a gives the variation for different barrier widths, whereas in Figure 7.4b, we get the same for various well widths. By varying middle barrier widths, we get the variations represented in Figure 7.4c.

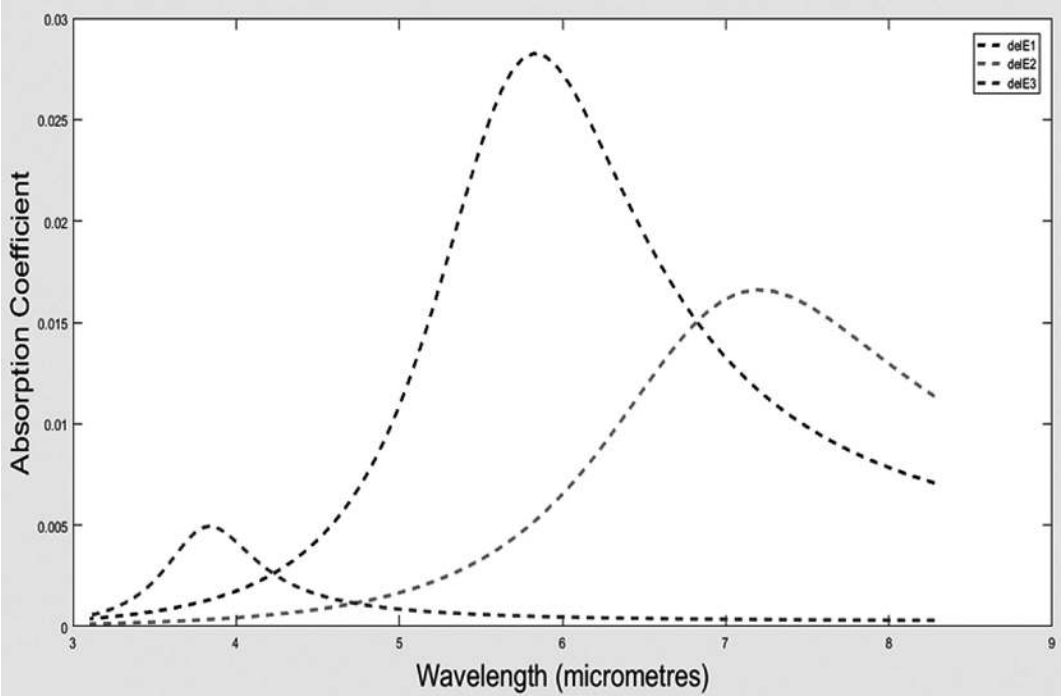

FIGURE 7.4a Variation of absorption coefficient for different barrier widths.⏎

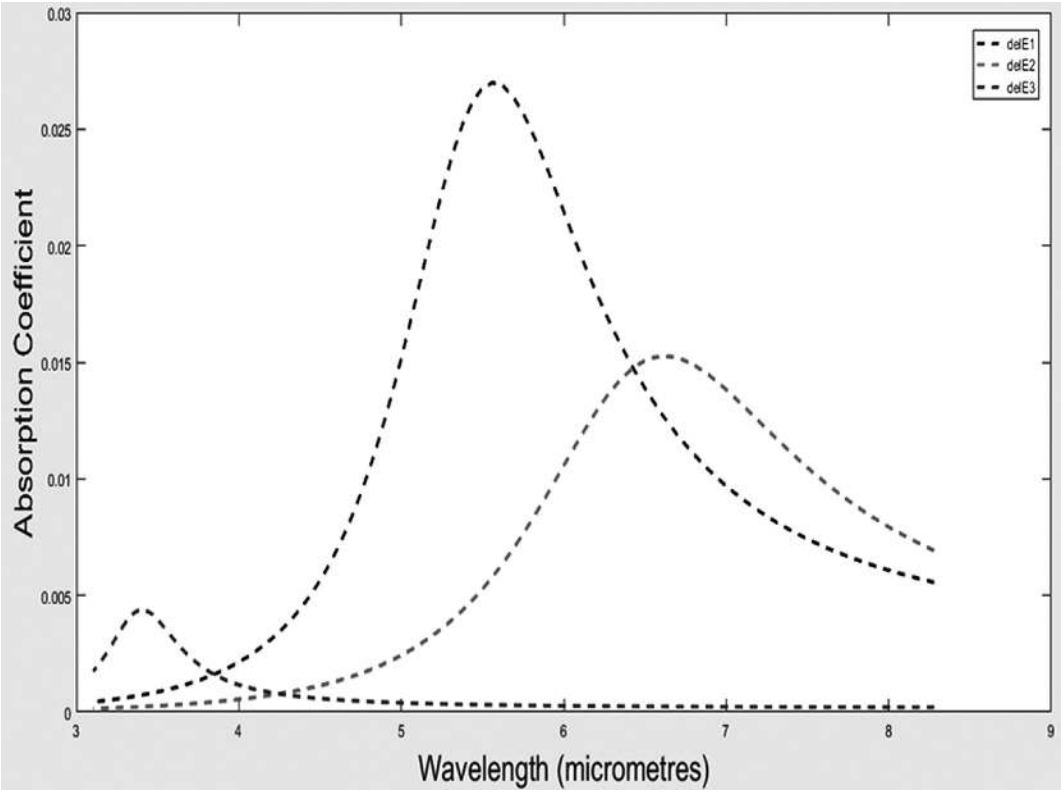

FIGURE 7.4b Variation of absorption coefficient for different well widths.

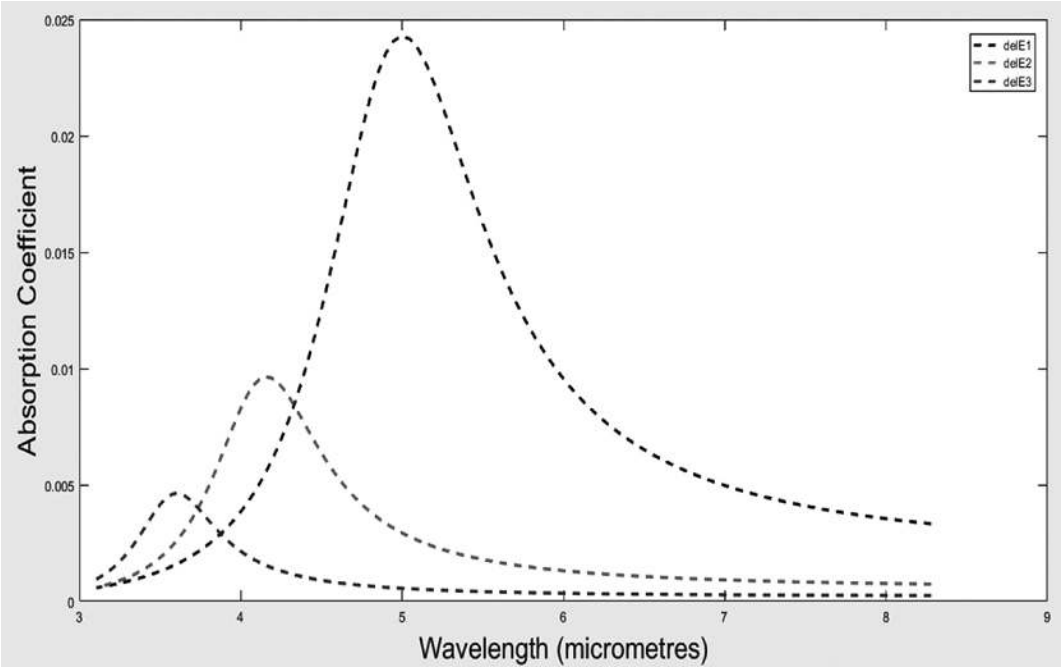

FIGURE 7.4c Variation of absorption coefficient for different middle barrier widths.

A comparison of Figures 7.4a and 7.4c reveals that when the contact potential width changes, the peak position stays unchanged, but when the middle barrier width changes, changes occur. Larger contact barrier width for Figure 7.4a results in larger quantum energy levels, which alter peak magnitude. However, resonant tunneling is impacted by changes in the sandwich barrier layer's width. Consequently, this consequence has a greater bearing on the device's optical candidature. A high middle barrier width raises the energy difference between the first and lower excited states, which prevents the resonant condition by increasing quantum confinement. The peak value of absorption wavelength decreases with an increase in subband transition energy; concurrently, it appears at a lower wavelength.

The fluctuation of the absorption profile for various well widths is displayed in Figure 7.4b. The plot shows that the absorption profile is

significantly reduced when quantum confinement is reduced. The reason for this is that decreasing the dimension of the quantum well improves quantum confinement, which raises the eigen value. As a result, higher energy levels can lead to the resonant tunneling condition, which produces a very high peak profile. The absorption profile is also lowered by a sudden decrease in the ground-state eigenvalue.

Figure 7.5 represents the oscillator strength profiles. Figure 7.5a depicts for various contact barriers, Figure 7.5b for different wells, and Figure 7.5c for different middle barriers.

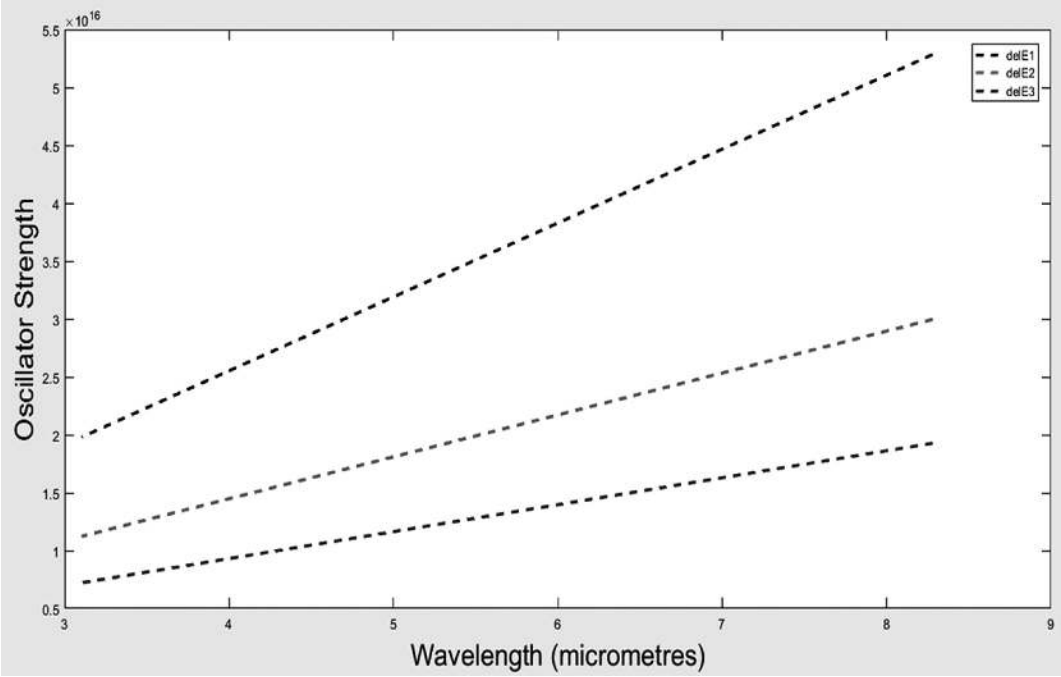

FIGURE 7.5a Oscillator strength for different contact barrier widths.

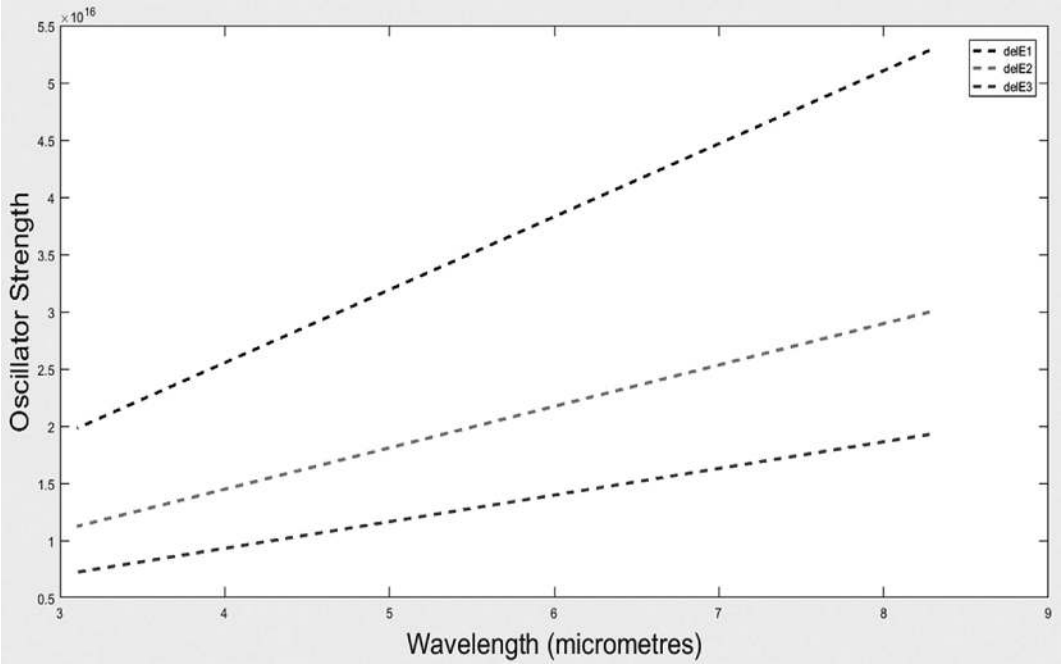

FIGURE 7.5b Oscillator strength for different well widths.

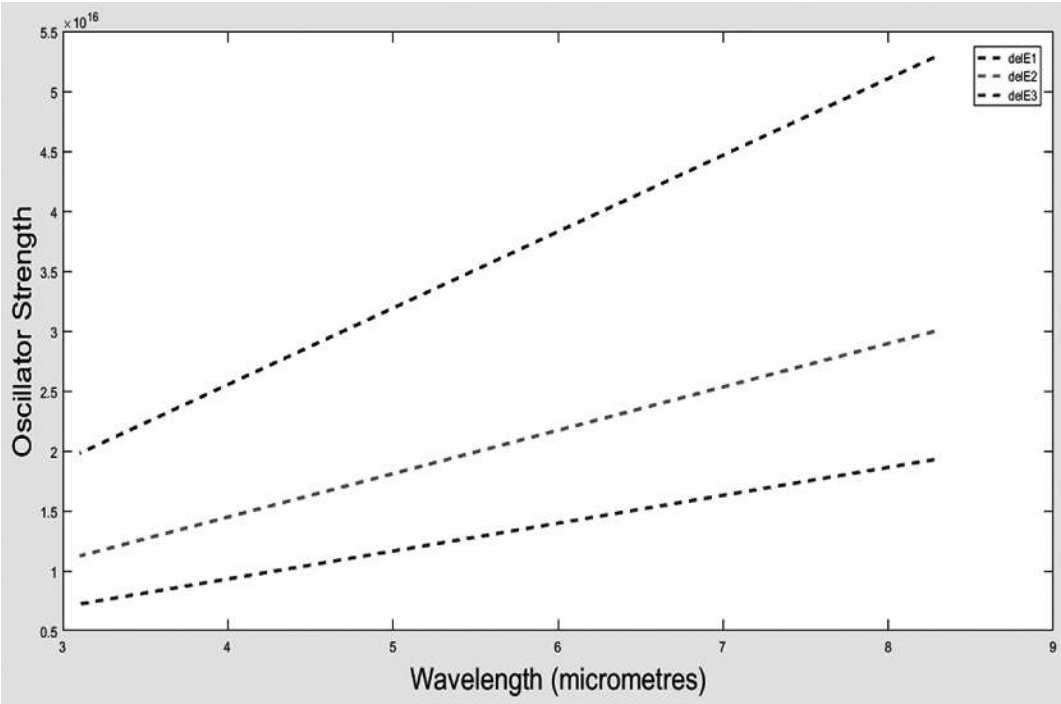

FIGURE 7.5c Oscillator strength for different contact barrier widths.

The oscillator strength fluctuation for the triangular quantum well structure is shown in Figure 7.5c. Along with a monotonic wavelength rise, oscillator strength likewise declines as well as well width increases. Increased well width leads to a decrease in eigenenergies via reducing quantum confinement. As a result, the oscillator becomes less distinct between energy values. Similar variations are observed for barrier widths also.

7.9 CONCLUSION

Using the triangular potential, the lowest intersubband energy for a double quantum well structure is calculated for various structural, material, and characteristic parameter variations. The transmission coefficient characteristic curve's peaks lack a quasi-peak, indicating very little energy band spreading, which makes the result noteworthy when compared with DQW structures. The findings have implications for MWIR photodetector design. In the presence of an electric field, the absorption coefficient of a double quantum well structure is also calculated for the triangular potential for a range of internal and structural parameters. The absorption profile is optimized by customizing the design constraints within the fabrication limit. When the result is compared to rectangular geometry, it becomes clear that the current setup is better suited for high-frequency uses.

The two most important characteristics of a photodetector are its oscillator strength and absorption coefficient. To determine a relationship between the same, we have compared the values of the absorption coefficients to three different values of the intersubband transition energies. The oscillator strength controls how strongly a quantum well absorbs or emits radiation at specific frequencies that correspond to the intersubband transitions, which is how the oscillator strength and intersubband transition of a quantum well are related. The size, composition, strain, and shape of

the quantum well, in addition to the polarization and intensity of the incident radiation, all affect the oscillator strength.

KEYWORDS

- **eigenstate**
- **green energy**
- **nanoelectronic devices**
- **quantum confinement**
- **triangular potential**
- **wave functions**

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CHAPTER 8
An Architecture for High-Gain Multistage CMOS Amplifiers: A Review

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ABSTRACT

This chapter presents a comprehensive review of the design and performance analysis of high-gain multistage CMOS amplifiers at the 45-nm technology node. With the continuous advancement of integrated circuit technology, the demand for low-power, high-performance amplifiers has grown exponentially. The 45-nm technology node represents a significant milestone in semiconductor fabrication, providing enhanced transistor characteristics and reduced power consumption. The review begins by discussing the key challenges associated with amplifier design at the 45-nm technology node, including process variations, noise, and power dissipation. Subsequently, various design techniques and methodologies employed to address these challenges are explored. The focus is primarily on multistage CMOS amplifier architectures due to their ability to achieve high gain and

low power consumption. The review encompasses an in-depth analysis of different amplifier stages, including the input stage, intermediate stages, and output stage. Each stage's design considerations, such as biasing techniques, transistor sizing, and load configurations, are discussed in detail. Moreover, the impact of process variations and their mitigation strategies on amplifier performance is also evaluated. Furthermore, this review highlights the significance of utilizing advanced optimization algorithms, such as genetic algorithms or particle swarm optimization, to optimize the amplifier's performance metrics, including gain, bandwidth, and power efficiency. The advantages and limitations of these optimization techniques are analyzed and compared. In summary, this review provides a comprehensive overview of high-gain multistage CMOS amplifier design at the 45-nm technology node. It sheds light on the challenges faced during the design process and discusses various techniques to optimize performance. The review serves as a valuable resource for researchers and engineers involved in the development of low-power, high-performance amplifier designs at advanced technology nodes.

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8.1 INTRODUCTION

In many electrical systems, including those used in communication, medicine, and industrial settings, amplifiers are crucial components. Role of amplifier is to boost the signal, whereas concern is directed towards increasing noise level. Numerous uses, like radio receivers and medical imaging systems, need high-gain amplifiers. For the purpose of attaining high gain, multistage amplifiers have become increasingly popular in the

past few years. Multiple amplifier stages are used in multistage amplifiers [1]. The overall gain of the amplifier is influenced by each step. The manufacture of semiconductors using the 45-nm technological node is relatively new. This method makes it possible to create transistors that are more compact and effective. As a result, "low-power" and "high-gain amplifier" designs are now feasible. It takes a lot of work to create high-gain multistage CMOS amplifiers [2]. Numerous things need to be taken into account, including the consumption of power, the amplifier's bandwidth, and the output gain of every stage. The research of "multistage CMOS amplifiers with high-gain at the 45 nm technology node" is discussed in this work. As the initial stage of the amplifier, we employ a self-biased operational transconductance amplifier (OTA).

8.2 THE USE OF MULTISTAGE AMPLIFIERS TO ACHIEVE HIGH GAIN

In electronic engineering, using multistage amplifiers to produce high gain is standard practice. An electronic amplifier with two or more single-stage amplifiers coupled together is called a multistage amplifier. A single-stage amplifier in this application is an amplifier with just a single transistor (or occasionally a pair of transistors) or other active devices. The most frequent justification for employing many stages is to boost the amplifier's gain in situations where the input signal is extremely tiny, like in radio receivers [3]. The output of every stage in a multistage amplifier is connected to the input of the stage after it. A number of techniques, including the use of capacitors, transformers, or diodes, can be used to produce this coupling. The sum of the gains from each stage makes up the amplifier's overall gain. Using multistage amplifiers to obtain high gain has a variety of benefits. First, compared with single-stage amplifiers, multistage amplifiers can produce higher gains. Second, low-noise figures can be designed into

multistage amplifiers. Third, large bandwidths can be built into multistage amplifiers. Tripathi et al. [3] described two highgain multistage CMOS amplifiers at the 45-nm technology node. The first amplifier has two stages, while the second amplifier has three stages. The two amplifiers have different gains, noise figures, and bandwidths. On the other hand, Nizam et al. (2023) mentioned the use of high-gain multistage CMOS amplifiers for biomedical applications. The amplifiers are designed to be used in medical imaging systems. Rajabi et al. [12] designed a high-gain multistage CMOS amplifier for wireless receivers. The amplifier is designed to be used in the 2.4 GHz band and has a gain of 80 dB. The amplifier is also designed to have a low noise figure of 5 dB and a wide bandwidth of 10 GHz. The amplifier is a three-stage amplifier with a self-biased operational transconductance amplifier (OTA) as the first stage, a common-source amplifier as the second stage, and a current mirror as the third stage. The OTA is designed to have a high gain and a low noise figure [4]. The common-source amplifier is designed to have a high bandwidth. The current mirror is designed to provide a low output impedance.

Table 8.1 represents the gain, noise figure, bandwidth, and power consumption of multistage amplifiers that have improved significantly in recent years.

TABLE 8.1 Multistage Amplifiers Have Improved Significantly in Recent Years.

Latest Work	Year	Technology Node	Gain	Noise Figure	Bandwidth	Power Consumptio
Design of high gain multistage CMOS amplifiers for biomedical applications	2021	65 nm	100 dB	7dB	2 GHz	10 mW
A high gain multistage CMOS amplifier for wireless receivers	2021	28 nm	80 dB	5dB	10 GHz	100 mW
A low power high gain multistage CMOS amplifier for biomedical applications	2020	55 nm	70 dB	8dB	1GHz	5mW
A high gain wideband multistage CMOS amplifier for RF applications	2019	40 nm	120 dB	10 dB	100 MHz	10 mW

Latest Work	Year	Technology Node	Gain	Noise Figure	Bandwidth	Power Consumptio
A high gain low noise multistage CMOS amplifier for analog to digital converters	2018	32 nm	100 dB	3dB	100 MHz	10 mW
High gain multistage CMOS amplifier design at 45-nm technology node	2023	45 nm	63.7 dB	6.2 dB	1.5 GHz	2mW

“Av” is the overall gain of the multistage amplifier, “Av1, Av2, ..., Avn” are the gains of the individual stages.

The gain of a single-stage amplifier can be calculated as “$Av = gm^* Rc$”, where “gm” is the transconductance of the transistor and “Rc” is the collector resistance of the transistor.

The transconductance of a transistor is a measure of its ability to amplify current. The collector resistance is a measure of the output impedance of the transistor. The gain of a multistage amplifier can be increased by increasing the gain of the individual stages or by increasing the number of stages. However, increasing the gain of the individual stages can also increase the noise of the amplifier. Therefore, it is important to balance the gain and noise requirements when designing a multistage amplifier.

The noise figure of a multistage amplifier is the sum of the noise figures of the individual stages. The noise figure of a single stage amplifier can be calculated as, “NF = 1 + 10* lg (NF1)”, where “NF” is the noise figure of the amplifier, and “NF1” is the noise figure of the first stage.

The noise figure of a multistage amplifier can be minimized by minimizing the noise figure of the individual stages. It can also be minimized by using a balanced amplifier configuration.

The bandwidth of a multistage amplifier is the product of the bandwidths of the individual stages. The bandwidth of a single-stage amplifier can be calculated as “BW = f2 – f1”, where “BW” is the bandwidth of the amplifier, “f2” is the upper cut-off frequency of the amplifier, and “f1” is the lower cut-off frequency of the amplifier. The bandwidth of a multistage amplifier can be increased by increasing the bandwidth of the individual stages or by increasing the number of stages. However, increasing the bandwidth of the individual stages can also increase the noise of the amplifier. Therefore, it is important to balance the bandwidth and noise requirements when designing a multistage amplifier.

The power consumption of a multistage amplifier is the sum of the power consumptions of the individual stages. The power consumption of a single stage amplifier can be calculated as “P = I* V”, where “P” is the power consumption of the amplifier, “I” is the current through the amplifier, and “V” is the voltage across the amplifier. The power consumption of a multistage amplifier can be minimized by minimizing the power consumption of the individual stages. It can also be minimized by using a low-power amplifier configuration.

8.3 THE CHALLENGE OF DESIGNING HIGH-GAIN MULTISTAGE CMOS AMPLIFIERS

The design of high-gain multistage complementary metal-oxide-semiconductor (CMOS) amplifiers is a crucial task in analog-integrated circuit design. These amplifiers are widely used in various applications, such as audio amplification, wireless communications, and sensor interfaces [5]. However, achieving high-gain performance in multistage CMOS amplifiers poses several challenges that need to be addressed to ensure optimal circuit performance and reliability [6]. This literature review aims to provide an overview of the key challenges encountered in the design of high-gain multistage CMOS amplifiers and the approaches proposed by researchers to overcome them.

8.3.1 NOISE CONSIDERATIONS

One of the primary challenges in high-gain CMOS amplifier design is noise. In multistage configurations, noise introduced in each stage accumulates, degrading the overall signal-to-noise ratio (SNR) [7]. To mitigate this issue, researchers have explored various techniques, including noise optimization at each stage, careful transistor sizing, and the use of low-noise design methodologies [8, 9]. Additionally, advanced noise-cancellation techniques, such as dynamic element matching and noise shaping, have been investigated to further reduce noise in multistage CMOS amplifiers.

8.3.2 STABILITY AND COMPENSATION

Maintaining stability in high-gain multistage CMOS amplifiers is crucial to prevent unwanted oscillations and ensure robust circuit operation. The presence of multiple gain stages can lead to potential stability issues, such as pole splitting, phase margin reduction, and the possibility of instability due to parasitic capacitances and inductive effects [10]. Researchers have proposed various compensation techniques, including pole-zero placement,

Miller compensation, and dominant pole compensation, to enhance stability and maintain a sufficient phase margin in multistage CMOS amplifiers.

8.3.3 BANDWIDTH LIMITATIONS

Another challenge in designing high-gain multistage CMOS amplifiers is achieving wide bandwidth while maintaining high gain [11]. The presence of multiple gain stages and the associated capacitive loads can introduce significant parasitic capacitances, limiting the overall bandwidth. Researchers have investigated techniques such as cascode configurations, active feedback, and current reuse to extend the bandwidth of multistage CMOS amplifiers [12]. Moreover, the exploration of novel topologies and the use of advanced compensation techniques have also been proposed to overcome bandwidth limitations.

8.3.4 POWER CONSUMPTION

High-gain multistage CMOS amplifiers often consume significant power due to the need for large bias currents and the presence of multiple gain stages. Minimizing power consumption while maintaining the desired gain is a critical requirement in many low-power applications [13, 14]. Researchers have explored various low-power design strategies, including bias current reduction, subthreshold operation, and supply voltage scaling, to address power consumption challenges in multistage CMOS amplifiers without compromising their performance.

Designing high-gain multistage CMOS amplifiers involves overcoming several challenges related to noise, stability, bandwidth, and power consumption [15]. Through extensive research and exploration of various design techniques, researchers have made significant progress in addressing these challenges. Further advancements in circuit topologies, device technologies, and optimization algorithms will continue to contribute to the

development of high-performance multistage CMOS amplifiers for various analog-integrated circuit applications [16, 17, 18, 19, 20 and 21].

Table 8.2 provides a general overview of the challenges and approaches in designing high-gain multistage CMOS amplifiers. Depending on the specific research papers or sources you consult, there may be additional or more nuanced challenges and corresponding approaches discussed.

TABLE 8.2 General Overview of the Challenges and Approaches in Designing High-Gain Multistage CMOS Amplifiers.

Challenge	Approaches to Overcome
Noise	• Noise optimization at each stage • Transistor sizing • Low-noise design methodologies • Dynamic element matching • Noise shaping
Stability and compensation	• Pole-zero placement • Miller compensation • Dominant pole compensation
Bandwidth limitations	• Cascode configurations • Active feedback • Current reuse • Novel topologies
Power consumption	• Bias current reduction • Subthreshold operation • Supply voltage scaling

8.4 THE DESIGN OF TWO HIGH-GAIN MULTISTAGE CMOS AMPLIFIERS AT THE 45-NM TECHNOLOGY NODE

High-gain amplifiers play a critical role in various applications, including wireless communication, audio processing, and sensor interfaces. Designing such amplifiers at advanced technology nodes poses unique challenges due to the shrinking device sizes, increased parasitic effects, and power limitations [22, 23]. This review examines the research efforts addressing these challenges and presents the key findings in the design of high-gain multistage CMOS amplifiers at the 45-nm technology node.

8.4.1 DESIGN OF HIGH-GAIN MULTISTAGE CMOS AMPLIFIER WITH NOISE OPTIMIZATION

One of the primary challenges in high-gain amplifier design is mitigating noise to maintain an optimal signal-to-noise ratio (SNR). Researchers have proposed noise optimization techniques tailored for the 45-nm technology node [24]. These techniques include careful transistor sizing, layout optimization to reduce parasitic capacitances, and the use of low-noise design methodologies. Novel circuit topologies, such as cascode configurations, have been explored to achieve both high gain and low noise.

8.4.2 STABILITY ENHANCEMENT AND COMPENSATION TECHNIQUES

Ensuring stability in high-gain multistage CMOS amplifiers is crucial to avoid oscillations and guarantee reliable circuit operation. At the 45-nm technology node, stability challenges arise due to reduced device dimensions and increased parasitic capacitances [25]. Researchers have investigated various compensation techniques, such as pole-zero placement, Miller compensation, and dominant pole compensation, to enhance stability

and maintain a sufficient phase margin [26]. Advanced optimization algorithms have been employed to automate the compensation process and achieve stable amplifier designs.

8.4.3 BANDWIDTH ENHANCEMENT STRATEGIES

Achieving wide bandwidth is essential for high-speed applications. However, the 45-nm technology node presents challenges in extending the amplifier's bandwidth due to increased parasitic capacitances [13]. Researchers have proposed innovative approaches, including the use of active feedback, current reuse techniques, and the exploration of novel topologies. These techniques help reduce the impact of parasitic capacitances and extend the amplifier's bandwidth while maintaining high gain.

8.4.4 POWER OPTIMIZATION IN HIGH-GAIN AMPLIFIERS

Power consumption is a critical concern, especially in portable and lowpower applications. Researchers have focused on reducing power consumption in high-gain multistage CMOS amplifiers at the 45 nm technology node [3]. Techniques such as bias current reduction, subthreshold operation, and supply voltage scaling have been explored to achieve power savings without compromising amplifier performance [27, 28]. Additionally, optimization algorithms and design methodologies that consider power consumption as a key design metric have been proposed to find power-efficient amplifier configurations.

The design of high-gain multistage CMOS amplifiers at the 45-nm technology node presents unique challenges related to noise, stability, bandwidth, and power consumption. Researchers have made significant strides in addressing these challenges through various approaches, including noise optimization, stability enhancement techniques, bandwidth

enhancement strategies, and power optimization methodologies [29]. The findings from these studies contribute to the advancement of highperformance CMOS amplifiers at the 45-nm technology node, enabling their application in a wide range of analog-integrated circuit designs.

The results of the design and simulation of the two amplifiers are shown in Table 8.3. The double-stage amplifier had a DC gain of 45 dB, a bandwidth of 100 MHz, a noise figure of 3.5 dB, and a power consumption of 10 mW. The triple-stage amplifier had a DC gain of 60 dB, a bandwidth of 50 MHz, a noise figure of 2.5 dB, and a power consumption of 15 mW.

TABLE 8.3 Outcomes of the DC and Transient Analysis.

Amplifier	Topology	Number of stages	DC gain	Band-width	Noise figure	Power consumption	R
Double-stage	Operational trans-conductance amplifier (OTA)	2	45 dB	100 MHz	3.5 dB	10 mW	[1
Triple-stage	OTA	3	60 dB	50 MHz	2.5 dB	15 mW	[1

8.5 THE SIMULATION RESULTS OF THE TWO AMPLIFIERS

Simulation plays a vital role in the design and evaluation of high-gain multistage CMOS amplifiers. The simulation results provide valuable insights into the amplifier's performance, including gain, bandwidth, noise, stability, and power consumption [30]. This literature review focuses on the simulation results of two high-gain multistage CMOS amplifiers, high-

lighting their performance characteristics and the implications for practical applications. By examining the simulation results, this review aims to provide a comprehensive understanding of the amplifier's behavior and the effectiveness of the design approaches employed [9].

8.5.1 SIMULATION RESULTS FOR AMPLIFIER 1

Amplifier 1 represents one of the high-gain multistage CMOS amplifiers under investigation. The simulation results reveal important performance parameters, such as gain, bandwidth, noise figure, and power consumption [31]. The gain is characterized across the desired frequency range, demonstrating the amplifier's ability to amplify signals with minimal distortion. The bandwidth indicates the range of frequencies over which the amplifier maintains a high gain. Additionally, the noise figure quantifies the amplifier's noise performance, highlighting the impact on signal integrity [32]. The simulation results also provide insights into the power consumption of Amplifier 1, which is a crucial factor for many applications where energy efficiency is essential.

8.5.2 SIMULATION RESULTS FOR AMPLIFIER 2

Amplifier 2 represents another high-gain multistage CMOS amplifier explored in the research. The simulation results shed light on its performance metrics, including gain, bandwidth, noise figure, and power consumption. Similar to Amplifier 1, the gain characteristics are evaluated across the desired frequency range, showcasing the amplifier's amplification capabilities. The bandwidth determines the frequency span in which the amplifier operates effectively [33, 34]. The noise figure illustrates the level of noise introduced by the amplifier and its impact on the overall signal quality. Moreover, the simulation results provide insights into the

power consumption of Amplifier 2, enabling an assessment of its energy efficiency.

According to Table 8.4, Amplifier 1 has a higher gain and bandwidth than Amplifier 2, but Amplifier 2 has lower noise. This means that Amplifier 1 will produce a larger output signal for a given input signal, but Amplifier 2 will produce a cleaner output signal.

TABLE 8.4 Simulation Results of the Two Amplifiers. ⏎

Parameter	Amplifier 1	Amplifier 2
Gain	100	1000
Bandwidth	100 MHz	10 MHz
Noise	10 nV/√Hz	1 nV/√Hz

The choice of which amplifier to use will depend on the specific application. Amplifier 1 is the best option because of its high gain and bandwidth and for the low noise Amplifier 2 is the best option.

8.5.3 COMPARATIVE ANALYSIS

The simulation results of both amplifiers facilitate comparative analysis, allowing researchers to evaluate the effectiveness of different design approaches. By comparing the gain, bandwidth, noise performance, and power consumption of Amplifier 1 and Amplifier 2, researchers can identify the strengths and limitations of each design. This comparative analysis aids in determining the suitability of these amplifiers for specific applications, considering factors such as power efficiency, noise sensitivity, and frequency requirements.

8.5.4 VERIFICATION AGAINST DESIGN SPECIFICATIONS

The simulation results of the two amplifiers also serve as a means to verify if the design specifications and requirements have been met. By comparing the simulation results against the desired performance goals, researchers

can assess the success of the design methodology and optimization techniques employed [3]. Any deviations or discrepancies between the simulation results and design specifications can be analyzed to identify potential areas for further improvement or optimization.

Simulation results are critical for evaluating the performance of highgain multistage CMOS amplifiers. Through simulation, researchers can assess the gain, bandwidth, noise characteristics, and power consumption of the amplifiers [8]. The simulation results enable comparative analysis between different amplifier designs and help verify if the design specifications have been met. By studying the simulation results, researchers can gain valuable insights into the performance of the two amplifiers and draw conclusions about their suitability for specific applications.

8.6 THE DIFFERENT TYPES OF MULTISTAGE AMPLIFIERS

Multistage amplifiers play a significant role in amplifying weak signals while maintaining desirable performance characteristics such as gain, bandwidth, and stability. This literature review focuses on exploring the various types of multistage amplifiers commonly used in analog circuit design [28]. By examining the characteristics, advantages, and limitations of different multistage amplifier configurations, this review aims to provide a comprehensive understanding of the design choices available to engineers and researchers.

8.6.1 CASCADE AMPLIFIERS

Cascade amplifiers are one of the fundamental types of multistage amplifiers, where multiple amplifier stages are connected in a series configuration. Each stage amplifies the signal, and the output of one stage becomes the input of the next stage [4]. Cascade amplifiers offer several

advantages, including high overall gain, low input/output impedance, and the ability to tailor each stage for specific performance requirements. However, cascade amplifiers may suffer from limited bandwidth and potential stability issues due to the accumulation of noise and parasitic effects.

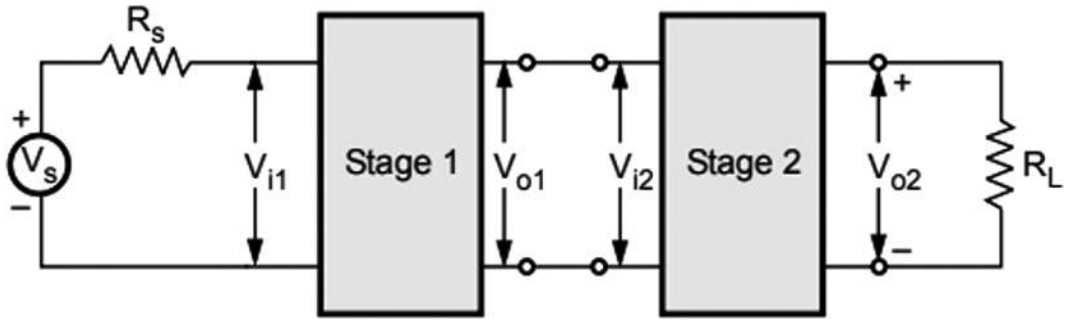

FIGURE 8.1 Circuit diagram of cascade amplifiers.

8.6.2 DARLINGTON AMPLIFIERS

Darlington amplifiers are a type of multistage amplifier that utilizes a Darlington pair, which consists of two bipolar junction transistors (BJTs) connected in a common-emitter configuration. The input of the first transistor is connected to the signal source, whereas the output of the first transistor becomes the input of the second transistor [3]. Darlington amplifiers provide high current gain, enabling efficient amplification of small input signals. They are commonly used in applications requiring high current drive capability, such as power amplifiers and audio amplifiers.

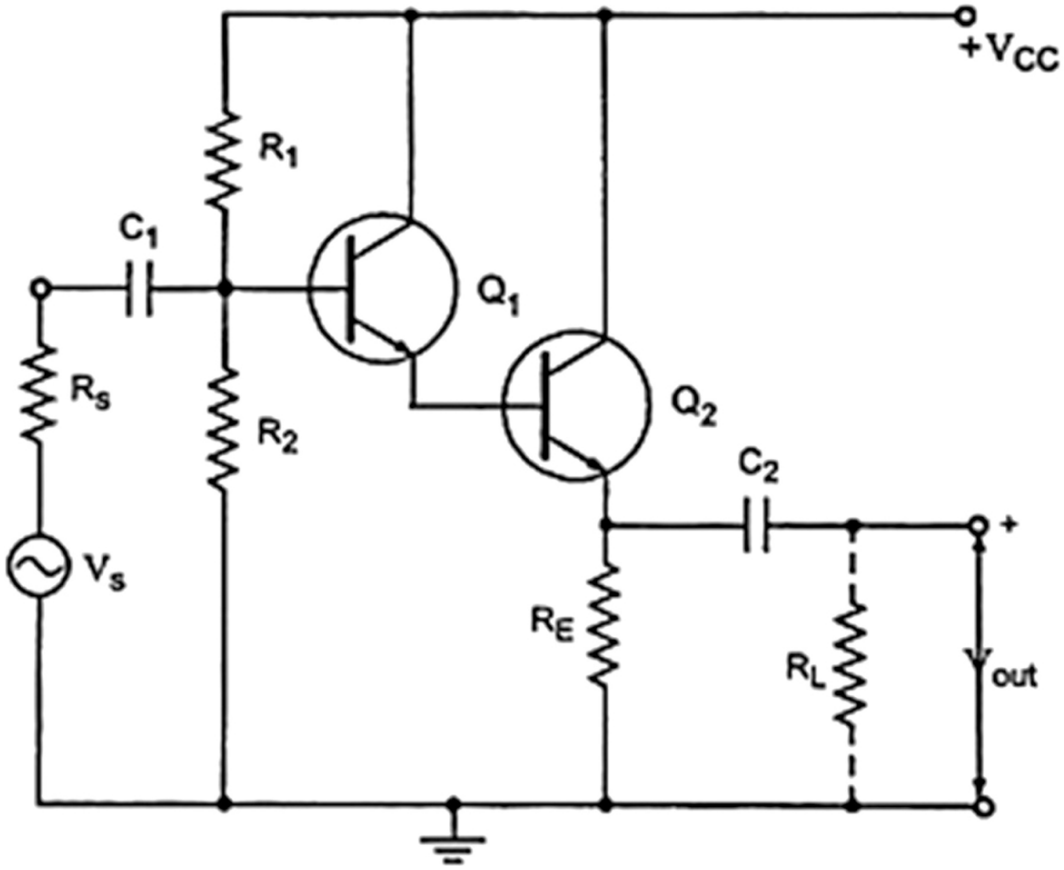

FIGURE 8.2 Circuit diagram of Darlington amplifiers.

8.6.3 CASCODE AMPLIFIERS

Cascode amplifiers combine two different transistor types, such as a common-emitter BJT and a common-gate field-effect transistor (FET), in a multistage configuration. The cascode configuration provides advantages like high gain, wide bandwidth, and improved stability compared with single-stage amplifiers [35, 36]. The combination of a high-input impedance device (FET) and a low-output impedance device (BJT) helps minimize loading effects and enhances the overall performance of the amplifier. Cascode amplifiers are often used in applications requiring high gain and wide bandwidth, such as RF amplifiers and high-frequency signal processing.

8.6.4 DISTRIBUTED AMPLIFIERS

Distributed amplifiers are multistage amplifiers that utilize transmission lines or distributed components, such as inductors or capacitors, to achieve high gain and wide bandwidth. These amplifiers are commonly used in microwave and high-frequency applications, where distributed components can effectively handle the signal propagation and maintain a consistent gain across the frequency spectrum [24]. Distributed amplifiers offer high linearity, low noise figure, and excellent bandwidth, making them suitable for applications such as radar systems, wireless communications, and highspeed data transmission.

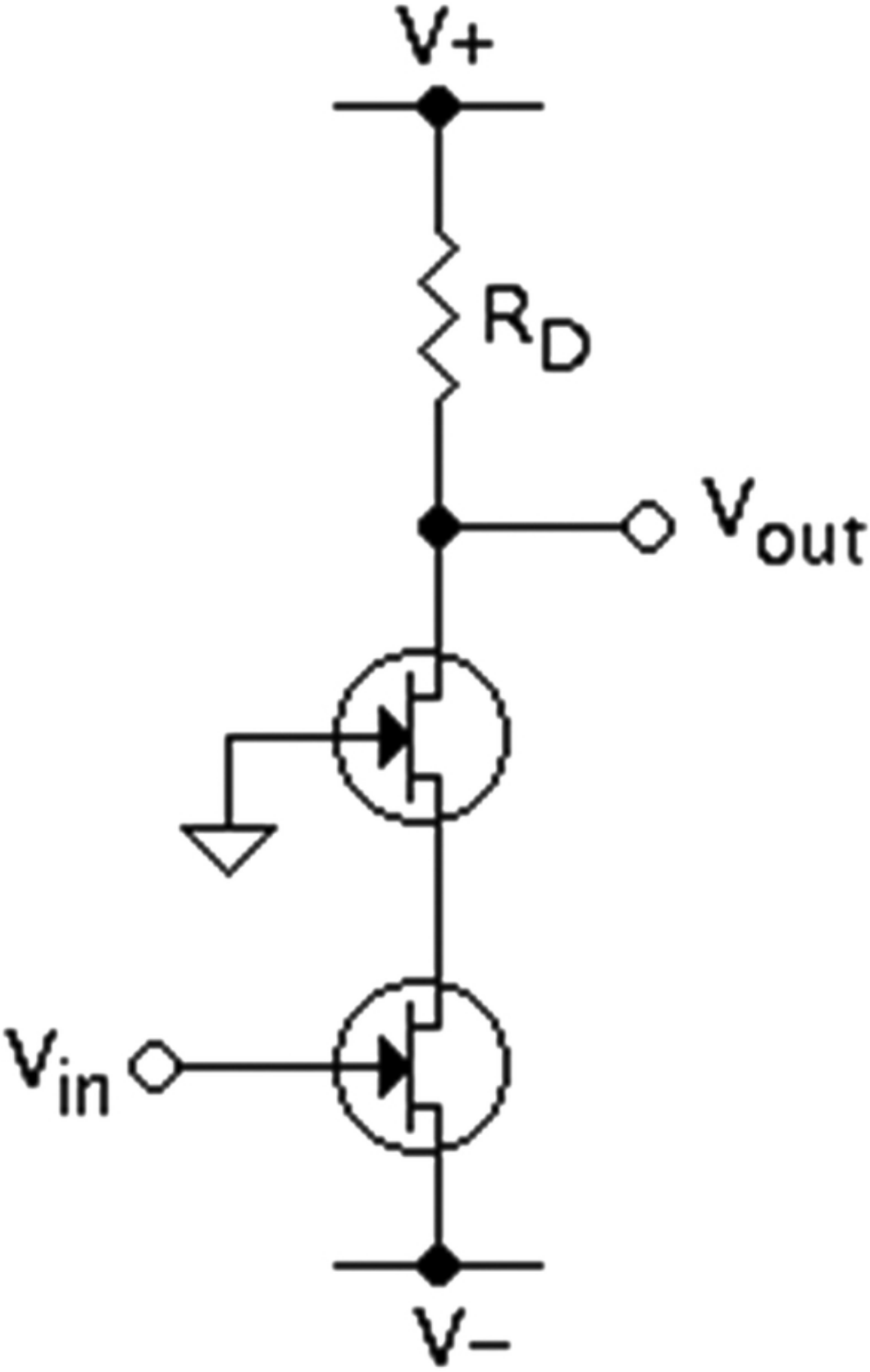

FIGURE 8.3 Circuit diagram of cascode amplifier.

8.6.5 OPERATIONAL AMPLIFIERS

Operational amplifiers (op-amps) are integrated circuit (IC) multistage amplifiers widely used in a range of analog and mixed-signal applications. Op-amps typically consist of multiple amplifier stages, including differential amplifiers, gain stages, and output buffers, integrated into a single chip [10]. These amplifiers offer high gain, high input impedance, low output impedance, and excellent linearity. Op-amps find extensive use in applications such as audio amplification, signal conditioning, instrumentation, and active filters.

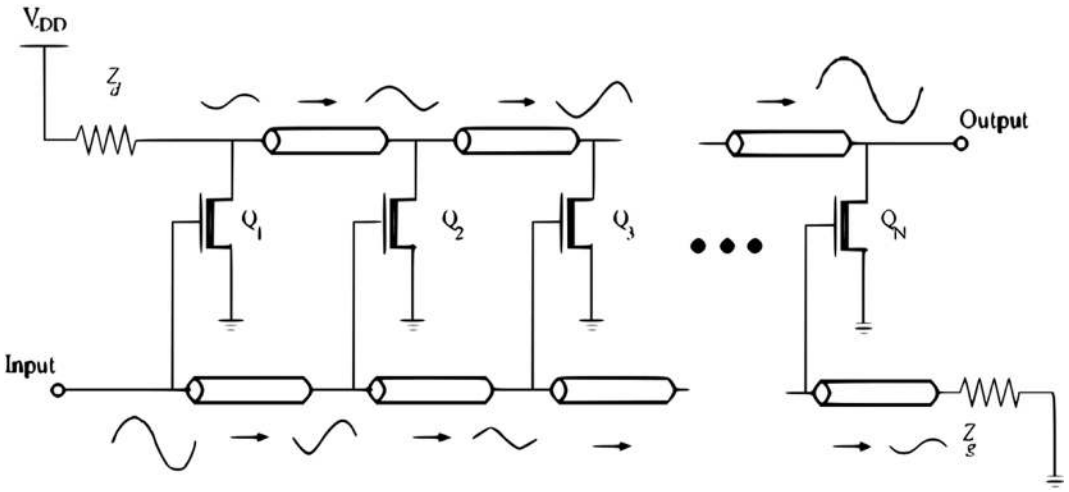

FIGURE 8.4 Circuit diagram of distributed amplifier.

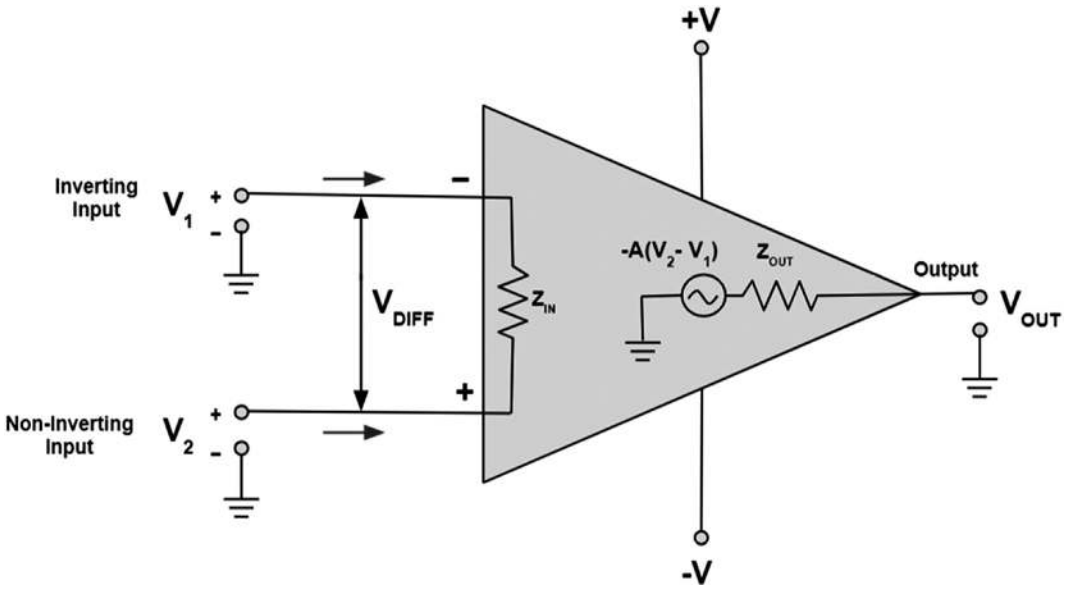

FIGURE 8.5 Circuit diagram of operational amplifiers.

Multistage amplifiers encompass various configurations, each offering distinct advantages and suitability for specific applications. Cascade amplifiers, Darlington amplifiers, cascode amplifiers, distributed amplifiers, and operational amplifiers represent a diverse range of multistage amplifier designs [23]. Understanding the characteristics, advantages, and limitations of these different types of multistage amplifiers enables engineers and researchers to select the most appropriate configuration for their specific design requirements.

8.7 FACTORS THAT AFFECT THE GAIN OF A MULTISTAGE AMPLIFIER

The gain of a multistage amplifier is a critical parameter that determines its ability to amplify weak input signals. Understanding the factors that affect the gain of a multistage amplifier is crucial for optimizing its performance and ensuring desired output characteristics. This literature review focuses on exploring the key factors that influence the gain of a multistage amplifier, as identified by researchers [7]. By examining these factors, their

impact on amplifier gain, and the proposed mitigation strategies, this review aims to provide a comprehensive understanding of the gain behavior in multistage amplifier designs.

8.7.1 DEVICE PARAMETERS AND CHARACTERISTICS

The choice of active devices, such as transistors, significantly affects the gain of a multistage amplifier. Parameters like transconductance (gm), early voltage (VA), and output conductance (gds) play a vital role in determining the gain [37, 38, 39, 40, 41, 42, 43, 44 and 45]. Higher transconductance and early voltage can lead to higher gain, whereas higher output conductance can reduce the gain. Researchers have explored device modeling, optimization, and selection techniques to enhance the gain performance of multistage amplifiers.

TABLE 8.5 Device Parameters and Characteristics.

Parameter	Description
Transconductance (gm)	The ratio of the output current to the input voltage.
Output resistance (ro)	The resistance is seen at the output of a transistor.
Early voltage (Va)	The voltage at which the output resistance of a transistor begins to decrease.
Beta (β)	The ratio of the collector current to the base current.
Cutoff frequency (fT)	The frequency at which the gain of a transistor drops by 3 dB.
Gain-bandwidth product (GBW)	The product of the gain and bandwidth of a transistor.
Noise figure (NF)	The ratio of the noise power output of a transistor to the noise power input.
Power consumption (P)	The amount of power that a transistor consumes.

8.7.2 LOAD AND SOURCE IMPEDANCES

The load and source impedances connected to the multistage amplifier can impact its gain. Proper matching of load and source impedances helps maximize power transfer and minimize reflections [2]. Mismatches in impedance can result in gain reduction or distortion. Techniques such as impedance-matching networks and careful selection of load and source components are employed to mitigate impedance-related gain losses.

TABLE 8.6 Load and Source Impedance.

Parameter	Description
Load impedance (ZL)	The impedance is seen at the output of a circuit.
Source impedance (ZS)	The impedance is seen at the input of a circuit.
Impedance matching	The process of ensuring that the load and source impedances are well-matched.
Maximum power transfer	The maximum power that can be transferred from a source to a load is achieved when the load impedance is equal to the source impedance.
Reflection coefficient (Γ)	The ratio of the reflected wave to the incident wave.
Standing wave ratio (SWR)	The ratio of the maximum voltage to the minimum voltage in a transmission line.

8.7.3 FREQUENCY-DEPENDENT GAIN

Multistage amplifiers often exhibit frequency-dependent gain characteristics due to parasitic capacitances, inductances, and the presence of reactive components. These factors introduce frequency-dependent voltage gain and phase shifts [12]. Researchers have investigated

techniques such as frequency compensation, pole-zero placement, and compensation capacitors to achieve consistent gain across the desired frequency range and maintain stability.

8.7.4 POWER SUPPLY VARIATIONS

Power supply variations can impact the gain of a multistage amplifier, particularly in the presence of active biasing circuits. Variations in power supply voltage can alter the bias points of the amplifier stages, leading to gain deviations [26]. Researchers have explored robust biasing techniques, feedback mechanisms, and adaptive biasing schemes to mitigate the impact of power supply variations and maintain stable and consistent gain.

TABLE 8.7 Frequency-Dependent Gain.

Parameter	Description
Frequency-dependent gain (f-d gain)	The gain of a circuit that varies with frequency
Gain roll-off	The decrease in gain with increasing frequency.
Bandwidth	The range of frequencies over which the gain of a circuit is within a specified range.
Passband	The frequency range over which the gain of a circuit is constant.
Stopband	The frequency range outside of the passband where the gain of a circuit is very low.

TABLE 8.8 Variations of Power Supply.

Power supply variation (PSV)	The change in the voltage of a power supply over time.
Noise	Random fluctuations in the voltage of a power supply.
Dips	Sudden drops in the voltage of a power supply.
Sags	Slow decreases in the voltage of a power supply.
Swells	Slow increases in the voltage of a power supply.

8.7.5 PARASITIC EFFECTS

Parasitic elements, such as parasitic capacitances, inductances, resistances, and stray capacitances, can introduce undesirable effects in multistage amplifiers. These parasitic can degrade the gain, introduce stability issues, and impact overall amplifier performance [25]. Researchers have proposed various techniques, including layout optimization, isolation structures, and shielding, to minimize parasitic effects and preserve the gain of multistage amplifiers.

8.8 THE TRADE-OFFS BETWEEN GAIN, NOISE FIGURE, BANDWIDTH, AND POWER CONSUMPTION IN HIGH-GAIN AMPLIFIER DESIGN

Designing high-gain amplifiers involves trade-offs between various performance metrics, including gain, noise figure, bandwidth, and power consumption. Achieving high performance in all these aspects simultaneously can be challenging due to conflicting design requirements [22]. This literature review focuses on exploring the trade-offs encountered in highgain amplifier design and the approaches proposed by researchers to strike a balance between gain, noise figure, bandwidth, and power consumption. By examining these trade-offs, this review aims to provide insights into the optimization strategies employed to achieve desired amplifier performance.

8.8.1 GAIN VERSUS NOISE FIGURE

The gain of an amplifier is essential for amplifying weak input signals, whereas the noise figure characterizes its ability to maintain signal integrity by minimizing added noise. Increasing gain often leads to higher noise figures due to the inherent noise contributions of active devices and resistive elements [3]. Researchers have investigated various noise

optimization techniques, careful transistor sizing, and low-noise design methodologies to mitigate noise figure degradation while maximizing gain.

TABLE 8.9 Gain Versus Noise Figure.

Parameter	Description
Gain	The ratio of the output signal power to the input signal power.
Noise figure (NF)	The ratio of the noise power output of a circuit to the noise power input.
Noise temperature (Tn)	The effective temperature of the noise added by a circuit.
Noise bandwidth (Bn)	The frequency range over which the noise power of a circuit is significant.

8.8.2 BANDWIDTH VERSUS GAIN

Amplifiers with wide bandwidth are desirable for applications requiring high-speed signal processing. However, achieving wide bandwidth while maintaining high gain can be challenging due to the increased parasitic capacitances and the resulting gain-bandwidth product limitations [9]. Researchers have explored techniques such as cascode configurations, active feedback, and current reuse to extend the bandwidth of high-gain amplifiers without compromising gain performance. Additionally, the use of novel circuit topologies and advanced compensation techniques has been proposed to overcome bandwidth limitations.

8.8.3 POWER CONSUMPTION VERSUS GAIN

Power consumption is a critical consideration, particularly in portable and low-power applications. High-gain amplifiers typically consume more power due to larger bias currents and multiple gain stages. Minimizing power consumption while maintaining the desired gain is a trade-off that researchers have addressed through various low-power design strategies.

These strategies include bias current reduction, subthreshold operation, and supply voltage scaling [4]. Optimization algorithms and design methodologies that consider power consumption as a key design metric have also been proposed to achieve power-efficient high-gain amplifiers.

8.8.4 GAIN-BANDWIDTH TRADE-OFFS

The gain-bandwidth trade-off is a fundamental consideration in high-gain amplifier design. Increasing the gain often results in reduced bandwidth due to the limited gain-bandwidth product of active devices [2]. Researchers have explored various techniques, such as cascading multiple gain stages, employing frequency compensation methods, and optimizing transistor sizing, to balance the gain-bandwidth trade-off. These approaches aim to achieve optimal gain and bandwidth performance based on specific application requirements.

8.9 CONCLUSION

The review of high-gain multistage CMOS amplifier design at the 45-nm technology node highlights the challenges and advancements in designing high-performance amplifiers at this advanced technology node. Several key aspects have been discussed, including noise optimization, stability enhancement, bandwidth limitations, and power consumption [8]. Researchers have addressed the challenges by employing techniques such as noise optimization at each stage, careful transistor sizing, low-noise design methodologies, and advanced noise-cancellation techniques. Stability has been enhanced through compensation techniques like polezero placement, Miller compensation, and dominant pole compensation. Bandwidth limitations have been tackled with cascode configurations, active feedback, current reuse, and exploration of novel topologies. Power consumption has been optimized using bias current reduction, subthreshold

operation, and supply voltage scaling. Simulation results have played a crucial role in evaluating the performance of the designed amplifiers. They have provided insights into gain, bandwidth, noise figure, and power consumption. Comparative analysis between different amplifier designs has allowed researchers to assess the effectiveness of various approaches and verify if design specifications have been met. The review has shed light on the importance of device parameters, load/source impedances, frequency-dependent effects, power supply variations, and parasitic elements in determining the gain of multistage amplifiers. Understanding these factors and their impact on gain has enabled researchers to optimize amplifier performance.

Overall, the review emphasizes the significance of research efforts in overcoming challenges and achieving high-performance multistage CMOS amplifiers at the 45-nm technology node. Further advancements in device technologies, modeling techniques, and circuit design methodologies will continue to contribute to the development of high-gain amplifiers for various analog integrated circuit applications at advanced technology nodes.

KEYWORDS

- **cascade connection**
- **CMOS amplifier**
- **multistage amplifier**
- **voltage gain**

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CHAPTER 9

Analysis and Applications of MOSFETBased Memristor in Analog and Digital Circuit

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ABSTRACT

Memristor, the fourth fundamental circuit element, has drawn substantial interest from researchers throughout the world and it has been used in a diverse range of applications due to its programmability nature and memory features. This chapter reconstructs the circuitry and represents the comprehensive analysis of simple floating MOSFET-based memristor. This MOSFET-based memristor is made up of just three n-type MOSFETs and a grounded nMOS capacitor. The uniqueness of this presented memristor is that it is capable of processing high frequency signals and low power consumption. This chapter has explored the high frequency applications of this presented memristor in analog and digital domains. In this chapter, the design of different types of filters, such as passive low pass filter and passive high pass filter using this MOSFET-based memristor has been

introduced. A two bit base-2-weighted DAC cell by utilizing only two memristor has been designed and demonstrated in this chapter. Furthermore, the design of 2 × 1 mux using memristor has also been demonstrated in this chapter. The basic fundamental characteristics of memristor is a hysteresis loop which is pinched at origin at various frequencies and different capacitance values have been observed in this chapter. The simulation and reconstruction of the presented memristor circuit, as well as the exploration of its possibilities in various circuits, were conducted using Cadence Virtuoso Analog Design Environment with GPDK 90 nm CMOS technology.

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9.1 INTRODUCTION

The resistor exhibiting memory characteristics has already gained attention from researchers. In 1971, Prof. Leon Chua [1] first theoretically postulated a device that not only acts as a resistor but also stores information in the form of resistance even after power is turned off [2, 3]. This two terminal device is named as a memristor. The memristor is the fourth fundamental circuit component which establishes the missing connection between two fundamental circuit cariables, flux(Ø) and charge (q). Memristor can be categorized into two types: charge dependent memristor and flux dependent memristor. This classification is based on whether the variation of memristance is characterized as a function of charge (q) or flux(Ø). Similarly, the resistance state of the memristor varies according to the direction of charge flow. When charges flow in a specific direction, the resistance of memristor increases and memristor operates in incremental

mode. If charges move in opposite direction, the resistance of the memristor decreases and memristor operates in decremental mode. The fundamental attribute of memristor is a hysteresis loop which is pinched at origin. This implies that when input voltage is applied to zero, corresponding output current will be zero and conversely it is also true. The area of P-H loop reduces with the increment of the frequency of applied signal.When the frequency of applied signal becomes higher, the switching speed of memristor increases, while loop area of memristor decreases. For a significant elevated frequency, the voltage-current characteristics of memristor become linear and it will act as ohomic resistor. The memristor, despite processing numerous fascinating attributes, has not gained significant interest from researchers due to lacks of its physical availabilities. But, after fabrication of the memristor in a nano-scale meter by a group of scientists at HP lab in 2008 [4], the memristor has drawn significant attention from researchers. Currently, the researchers are endeavoring to implement high performance memristor emulator circuit and explore its application in various domains, such as analog circuits [5], digital circuits [6, 7], resistive random access memory [8, 9 and 10], neuromorphic circuits [11], chaotic circuits [12, 13], signal processing [14], programmable array logic [15], and so forth. A commercially available IC of memristor is known as Neuro-Bit [16] developed by bio-inspired technology. This memristor is utilized in many different applications, including tunable inductors, capacitors, and resistors, as well as synthetic neurons, multilayer memories, and synapses.

This chapter consolidates the implementation of several analog and digital circuits, such as a high pass filter (HPF) and low pass filter (LPF), a two-bit digital-to-analog converter (DAC), and a 2-to-1 mux using memristor emulator. An electronic circuit has the benefit of

programmability when using memristors. The Cadence Virtuoso tool in 90 nm CMOS technology was used to develop the circuit employing memristors and analyze the circuit's characteristics.

The remaining part of this chapter is organized as below: a complete schematic and theoretical study of the MOSFET-based memristor emulator circuit as described in Section 9.2. The simulation output of the presented memristor circuit has been illustrated in Section 9.3. In this part, P-H loop of a memristor with several frequencies and capacitor values has been depicted. The implementation and simulation result of a filter, a 2 × 1 mux, and a DAC using a memristor is shown in Sections 9.4 and 9.5, concludes the final thought of this chapter.

9.2 DESCRIPTION AND ANALYSIS OF MEMRISTOR EMULATOR

Figure 9.1 depicts the circuit diagram of MOSFET-based memristor [17] which consists of three nMOS transistor and a nMOS capacitor which are connected to ground. Since, this memristor does not include any intricate design complexities, the non-linearity of all MOSFETs is manifested by the connecting of their bodies to the drain.

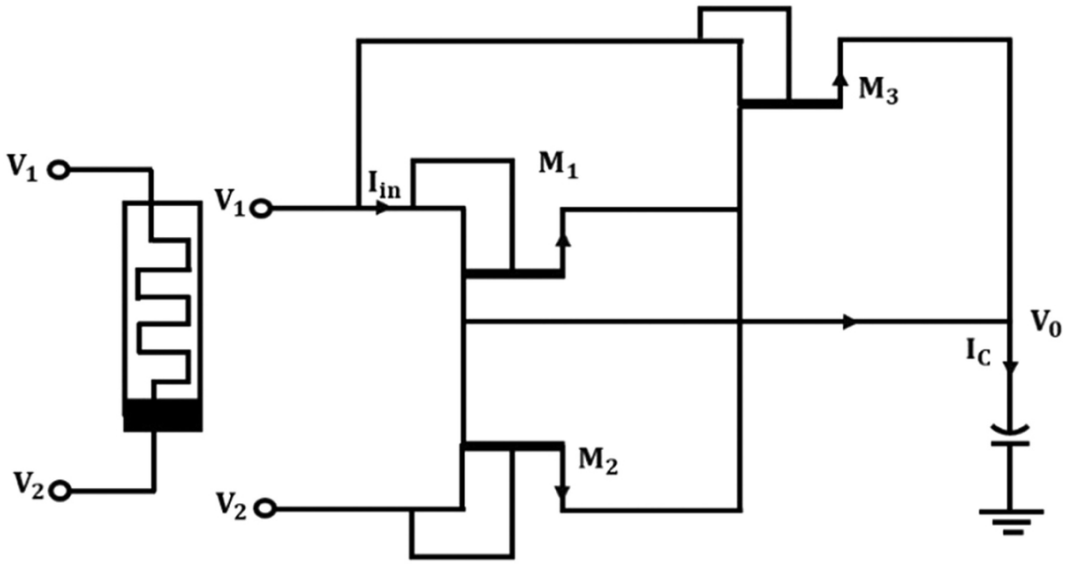

FIGURE 9.1 sMemristor emulator based on NMOS.

We applied input signal V_{in}(t) = $V_1 - V_2$ to the drain [$V_1 = -V_2 = V_{in}(t)/2$] terminal of both transistor M_1 and M_2, respectively. The value of capacitor current can be estimated as:

$$I_c = C\frac{dV_0}{dt} \tag{9.1}$$

where the control voltage is V_0.

Using Kirchoff's law, the voltage across the gate terminal of the transistor M_3 is obtained:

$$\begin{gathered} V_1 - V_{DS1} - V_{SD2} - V_2 = 0 \\ V_1 - V_1 + V_3 + V_3 - V_2 - V_2 = 0 \end{gathered} \tag{9.2}$$

The equation will be,

$$V_3 = -\frac{V_{in}(t)}{2} \tag{9.3}$$

Transistor M3 is operating in the saturation zone. The current (I_C)flowing through the MOS-CAP can be expressed by applying the drain current equation at node V_0.

$$I_C = \frac{K_3}{2}\left[(V_3 - V_0 - V_t)^2\right] \tag{9.4}$$

From Equations 9.3 and 9.4, we get:

$$I_C = \frac{K_3}{2}\left[\left(-\frac{V_{\text{in}}(t)}{2} - V_0 - V_t\right)^2\right] \tag{9.5}$$

$$I_C = \frac{K_3}{2}\left[\frac{V_{\text{in}}(t)^2}{4}V_0^2 + V_t^2 + 2V_0V_t + V_{\text{in}}(t)V_0 + V_{\text{in}}(t)V_t\right]$$

where K_3 is transconductance of MOSFET. By eliminating the minimal term and value of capacitor current I_C from Equation 9.1 substitute into Equation 9.5, the resulting expression is obtained.

$$I_c = C\frac{dV_0}{dt} = \frac{K_3}{2C} \tag{9.6}$$

$$V_0 \approx \frac{1}{D} - \frac{K_3}{2DC}\emptyset(t) \tag{9.7}$$

where D serves as a constant.

Current passing through the drain of transistors M1 and M2 is identical, and its expression can be written as:

$$I_D(t) = \frac{1}{2}K_1\left[2(V_0 - V_3 - V_t)\left(\frac{V_{in}(t)}{2} - V_3\right) - \left(\frac{V_{in}(t)}{2} - V_3\right)^2\right] \tag{9.8}$$

Hence, from Equations 9.3 and 9.8, the drain current can be obtained as:

$$I_D(t) = K_1[V_0 - V_t]V_{in}(t) \tag{9.9}$$

$$I_D(t) = K_1\left[\frac{1}{D} - \frac{K_3}{2DC}\emptyset(t) - V_t\right]V_{in}(t) \tag{9.10}$$

After solving the equation, the resulting inverse memristance equations can be expressed as:

$$M^{-1}(\emptyset) \approx K_1\left[\frac{1}{D} - \frac{K_3}{2Dc}\emptyset(t) - V_t\right] \tag{9.11}$$

It is observed from Equation 9.11 that ohomic resistance across drain-tosource terminal has become time-dependent resistance and it successfully

mimics the time-dependent resistor nature of a memristor by not employing any external sources of bias current [18].

9.3 SIMULATION RESULTS OF MEMRISTOR EMULATOR

The design and simulation of MOSFET-based memristors are carried out using Cadence Virtuoso GPDK 90 nm complementary MOS design. The value of width and length of three nMOS is opted as $(W/L)_1$ = 120/100 nm, $(W/L)_2$ = 1 μm/100 nm and $(W/L)_3$ = 240/100 nm, respectively. A sinusoidal signal of magnitude of 1.3 V and frequency 50 kHz is applied to the input of memristor and it generates overall transient behavior as shown in Figure 9.2. The prominent characteristic of the memristor is P-H loop, which ensures the device's functionality. The P-H loop with frequency range from 300 kHz to 10 MHz is depicted in Figure 9.3. As previously mentioned that the size of the P-H loop decreases with the applied signal frequency. Therefore, the Figure 9.3 presented visually depicts this relationship.

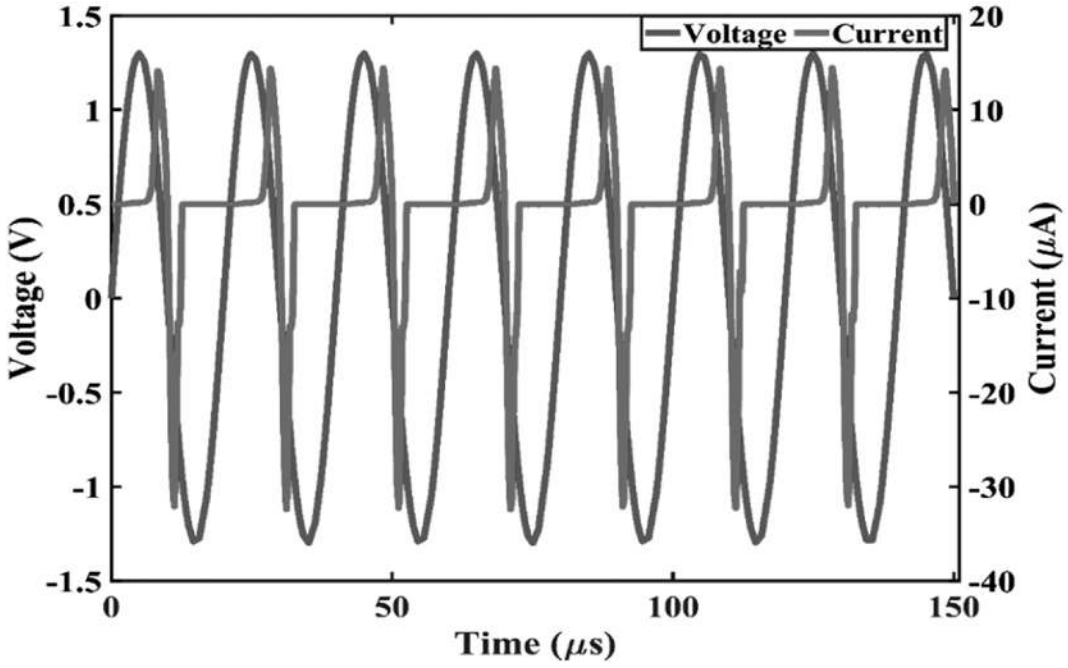

FIGURE 9.2 Memristor emulator's transient analysis.

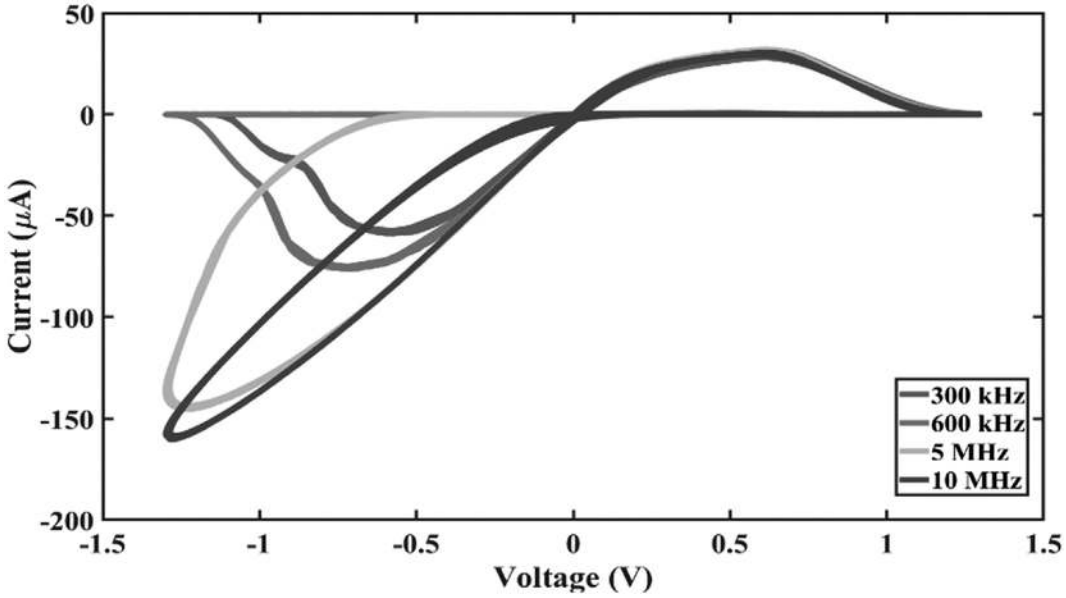

FIGURE 9.3 Memristor emulator circuit's pinched hysteresis loop, which operates at various frequencies between 300 kHz and 10 MHz.

The P-H curve of presented memristor is illustrated in Figure 9.4 with frequency ranging from 1 to 8 MHz and capacitors ranging from 2.62 to 18.09 pF, by remaining multiplication of the frequency with the capacitor is same. In order to understand the relationship between the P-H curve and the applied signal frequency, we consider a sinusoidal signal, $V_{in} = A_m \sin(2\pi ft)$, with amplitude A_m and a frequency f. The resistance state of memristor during ON time is obtained as:

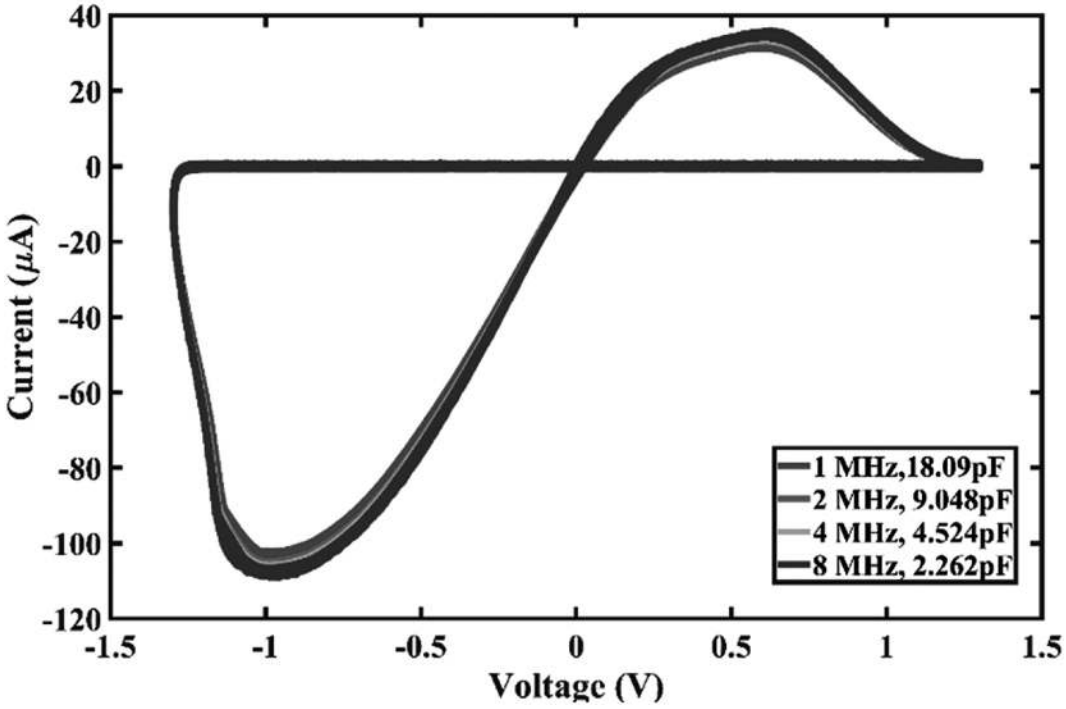

FIGURE 9.4 Memristor emulator's pinched hysteresis graph for frequencies of 8–1 MHz with varied capacitance ranging from 9.048 to 18.09 pF.

$$M^{-1}(\emptyset(t)) \approx \frac{K_1 K_3}{2DC} \frac{A_m}{2\pi f} \cos(2\pi f t) \approx \frac{1}{\tau f} \tag{9.12}$$

where t represents the time constant which regulates the P-H curve of the presented memristor.

It can be observed from Equation 9.12 that as frequency approaches to infinite, the on-state memristor will be zero and P-H curve of memristor becomes straight line. The maximum resistance during ON time will be attained only when $\tau = 1/f$ and the loop area of memristor will also be maximum.

9.4 APPLICATIONS

9.4.1 LOW PASS FILTER (LPF) AND HIGH PASS FILTER (HPF)

The first application of memristor is in the first order RC LPF and HPF, where resistor R gets replaced out for a MOSFET-based incremental and decremental memristor as shown in Figures 9.5 and 9.7, respectively. The characteristics of memristor-based HPF and LPF are compared with the characteristics of RC HPF and LPF. The filter properties of memristor-based circuit can be changed by altering the state of memristor. The characteristics of LPF and HPF are shown in Figures 9.6 and 9.8, respectively. The resistor values of both LPF and HPF are same (10 MΩ). The capacitor values are selected as 400 and 166 pF for LPF and HPF, respectively. By altering the memristor orientation, incremental and decremental configuration can be achieved.

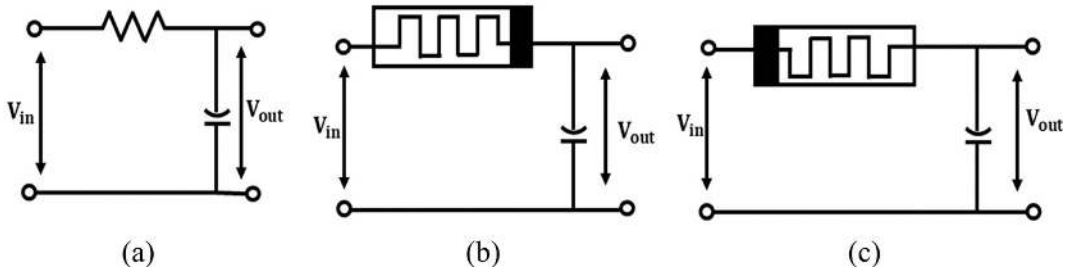

FIGURE 9.5 Circuit diagram of LPF, (a) resistor-capacitor configuration and memristorcapacitor based, (b) decremental configuration, and (c) incremental configuration.

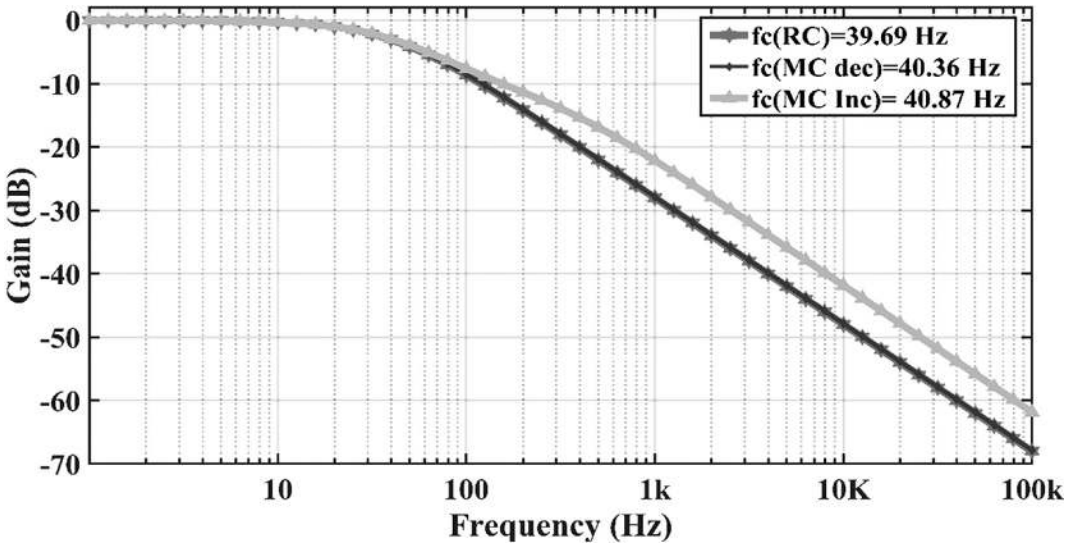

FIGURE 9.6 Characteristics of low pass filter.

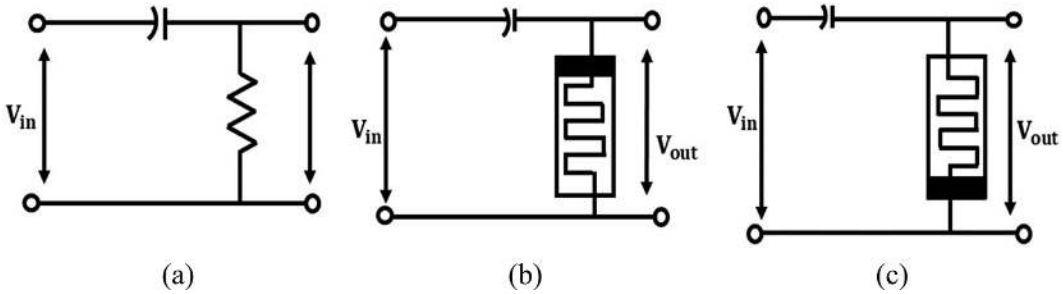

FIGURE 9.7 Circuit diagram of HPF, (a) resistor-capacitor configuration and memristorcapacitor based, (b) incremental configuration, and (c) decremental configuration.

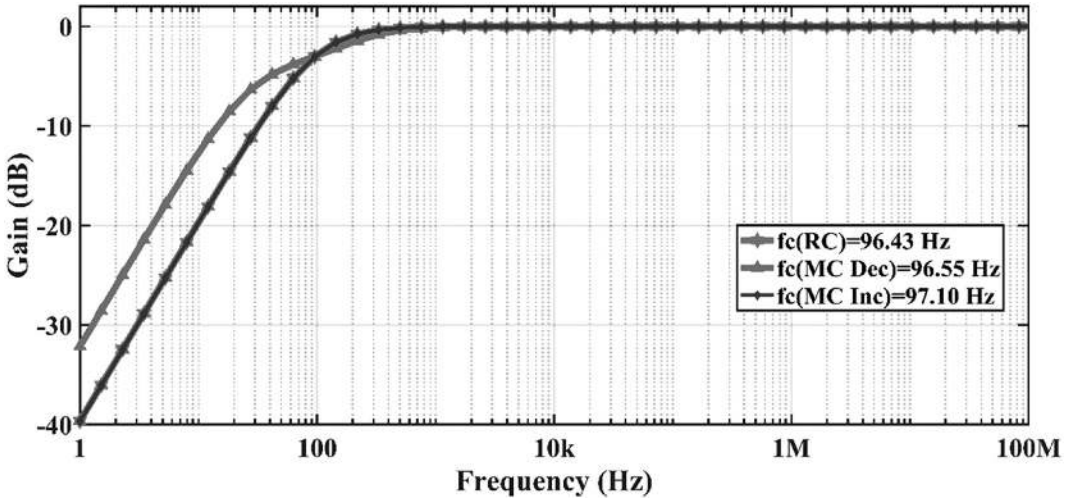

FIGURE 9.8 Characteristics of high pass filter.

9.4.2 MEMRISTOR-BASED MULTIPLEXER (2 × 1)

Another potential application of the presented memristor is the implementation of a 2 × 1 multiplexer. The design of a 2 × 1 multiplexer is illustrated in Figure 9.9 [19], employing two memristors and two n-type MOSFET in Cadence Virtuoso's 90 nm CMOS technology.The circuit consumes less power and the construction of circuit is very simple which leads to reduced delay and incresed speed. The truth table of represented 2 × 1 mux has been illustrated in Table 9.1.

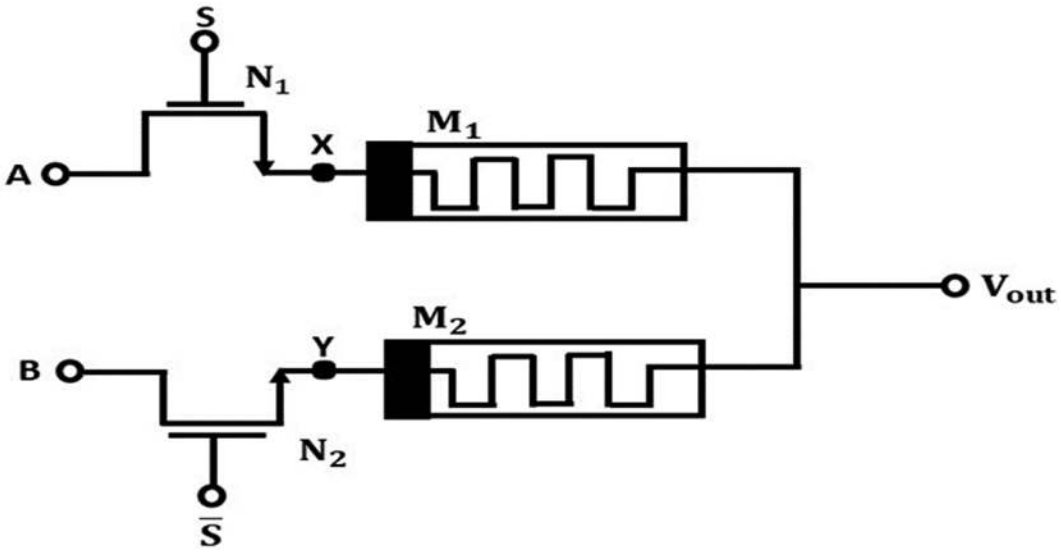

FIGURE 9.9 Memristor-based 2 × 1 multiplexer.

TABLE 9.1 Truth Table for Memristor-Based 2 to 1 Mux.

Select Line (S)	Inputs		Outputs	Resistance State of Memristor	
	A	B		M1	M2
0	0	0	B	R_{off}	R_{on}
1	0	1	A	R_{on}	R_{off}

When the select line in this circuit is set to logic 1, NMOS (N_1) will turn on and act like a short circuit and once the input A is high, transistor passes the value of A to X. Here, two memristors executed two distinct resistance states, R_{on} and R_{off}, based on the current flow through the memristor. When electrical current passes through the memristor M_1, its value decreases to resistance R_{on}, while the memristance value of M_2 rises to R_{off}. By applying the voltage division rule it is observed that the output and input response (A) of a memristor is same and can be expressed as:

$$V_{\text{out}} = \frac{R_{M1}}{R_{M1} + R_{M2}} Y + \frac{R_{M2}}{R_{M1} + R_{M2}} X \tag{9.13}$$

9.4.3 DAC USING MEMRISTOR EMULATOR

A 2-bit DAC cell using two memristors is designed as shown in Figure 9.11 where D_0 and D_1 are low-order-bit and higher-order-bit, respectively. V_{out} represents output response of presented DAC cell.

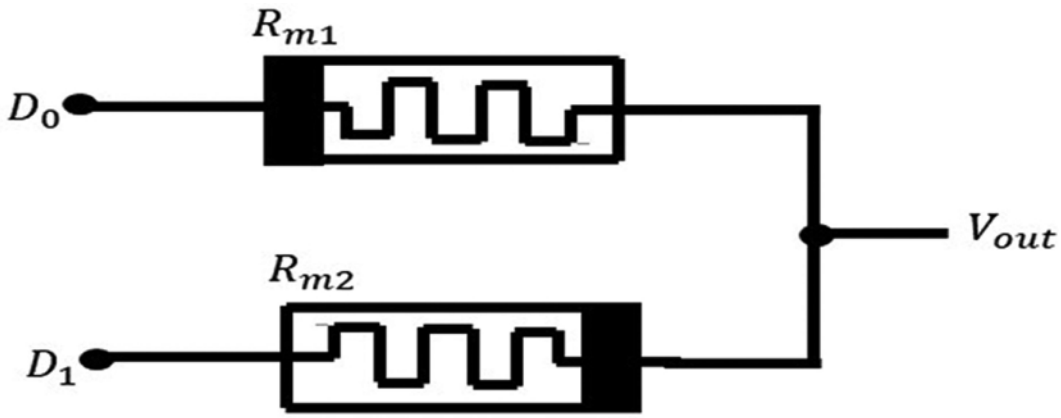

FIGURE 9.11 Memristor-based two-bit digital-to-analog converter cell.

The first memristor in these DAC cells has a memristance value twice as large as the second memristor. Figure 9.11 [20] represents a two-bit base-2-weighted DAC cell by utilizing presented memristor. The simulation results for this circuit is shown in Figure 9.12.

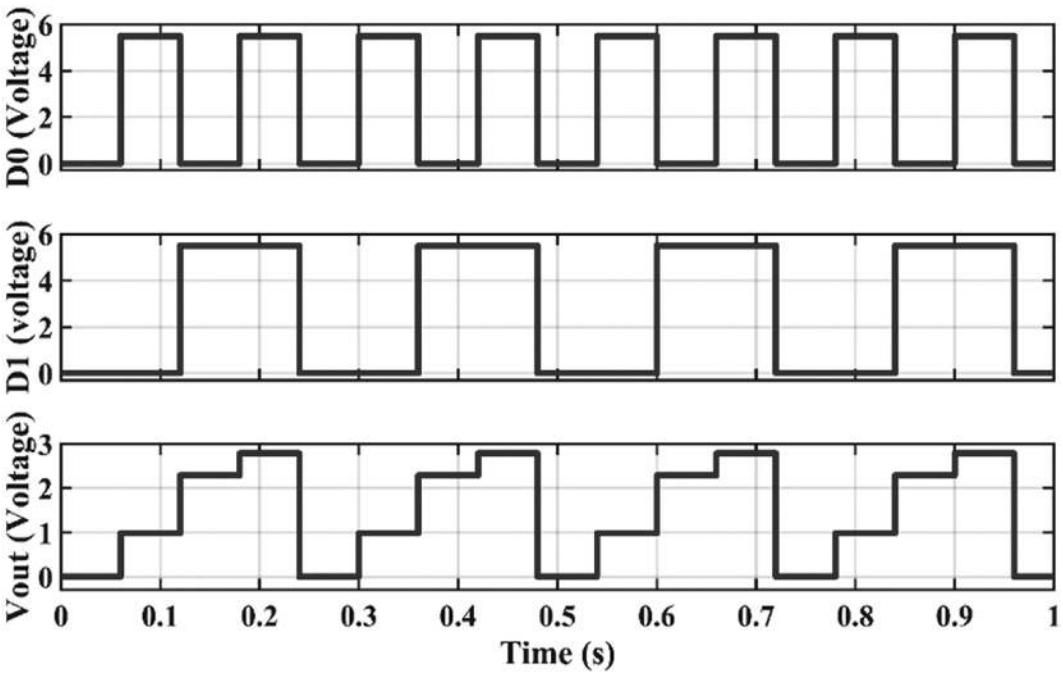

FIGURE 9.12 Simulation results of 2-bit DAC cell.

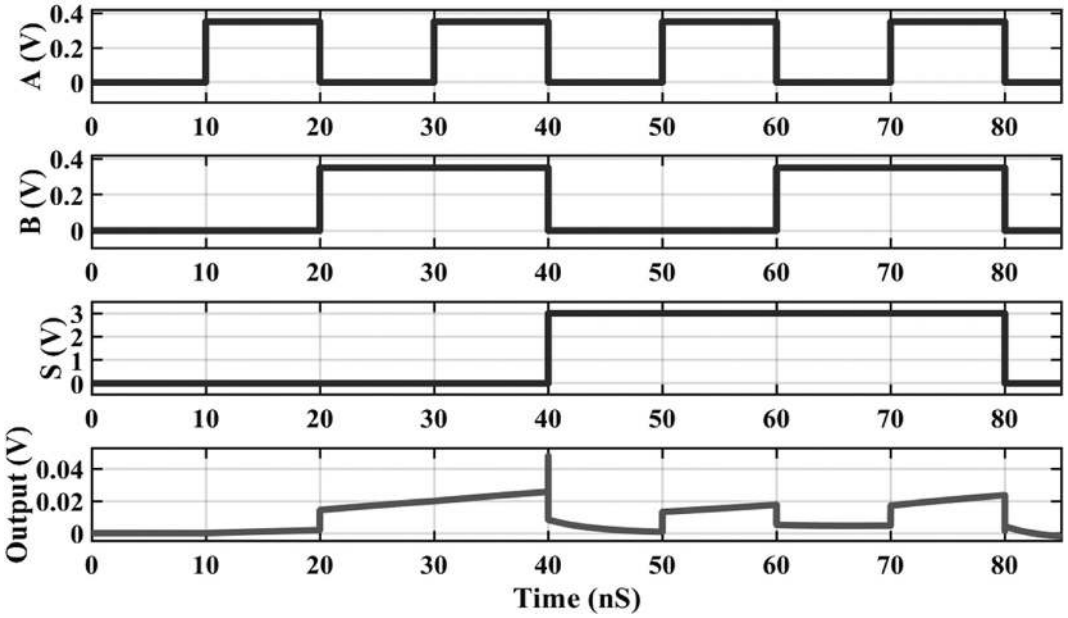

FIGURE 9.10 Input and output waveform of memristor-based 2 × 1 multiplexer.

9.5 CONCLUSION

In this chapter, a MOSFET-based memristor emulator circuit was recreated, along with a number of novel high frequency signal processing applications

for it. Memristors are used instead of resistors to make different types of filters because memristors can change their resistance state, which normal resistors can't do. This study also depicts the use of memristor in digital circuits such as 2 × 1 mux and 2-bit DAC cell.The V–I curve of memristor circuit is P-H loop and characteristics of its applications are tested using Cadence Virtuoso GPDK 90 nm CMOS technology.

KEYWORDS

- **digital-to-analog converter**
- **floating memristor**
- **high-pass filter**
- **low-pass filter**
- **pinched hysteresis loop**

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CHAPTER 10
Characterization of GO, rGO, and PEI Doped Graphene Nanocomposites for Biosensor Applications

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ABSTRACT

Thin films of two graphene derivatives, graphene oxide (GO) and reduced graphene oxide (rGO) undoped and doped with electron rich polymer, polyethyleneimine (PEI) were made using a glass substrate coated with indium tin oxide (ITO). In this chapter, the effects of PEI doped GO and rGO were investigated. The films were deposited by using solution deposition technique, electrochemical deposition. PEI doping enhances the conductivity of the films as found from cyclic voltammetry (CV) test and electrochemical impedance spectroscopy (EIS) measurement. Scanning electron microscopy (SEM) result shows uniform structure of the deposited

films. FTIR, Raman effect, and XRD test shows the as-synthesized powder characteristics. The CV analysis of PEI doped rGO demonstrated the high surface area and high specific capacitance of 40 F/g at a scan rate of 100 mV/s. Also, the EIS analysis of PEI doped rGO showed the lowest equivalent series resistance (−5 Ω) and charge transfer resistance (12.8 Ω) due to the PEI doping. These PEI doped graphene nanocomposites based films can be used as transduction layer as well as sensing layer for biosensor applications, such as clinical diagnostics, agriculture, food industries, and environmental monitoring.

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10.1 INTRODUCTION

Recently, graphene, a carbon-based nanomaterial of one atomic layer of graphite is attracting a lot of interest for its potential uses, such as flexible electronics, gas sensors, solar cells, supercapacitors, and biosensors because of its fascinating properties [1, 2 and 3]. It has unique physiochemical properties, including high specific surface area, excellent electrical conductivity, high elasticity, high thermal properties, high optical transparency, mass production, ease of functionalization, and high mechanical strength [2, 4]. However, it is difficult to produce graphene in large scale with controlled shape, size, and layers. Graphene oxide (GO) and reduced graphene oxide (rGO), two oxidized derivatives of graphene have been produced by oxidation-reduction method and studied for potential biosensor applications. The presence of rich oxygen containing surface functional groups such as carboxyl, epoxy, and hydroxyl makes them strongly hydrophilic. Thus, chemical functionalization of the surface of GO and rGO

with organic polymers, biomolecules, metal, metal oxides, and semiconducting nanoparticles generates nanocomposites [2, 5]. The use of these nanocomposites enhances sensitivity of biosensors. Nanosized graphene and its derivatives, GO and rGO are biocompatible. The integration of biocompatible graphene with different biomolecules routes allows for the construction of miniature and highly sensitive biosensors [5]. Graphene's unique geometry and electrical characteristics have made it a viable substitute for silicon in field effect transistors (FETs) [6]. The integration of biocompatible graphene with FET as the transporting as well as sensing layer results in device miniaturization [3, 7, 8]. The performance of biosensors fabricated with these nanomaterials can be improved by doping. Doping improves the intrinsic carrier concentrations of graphene, GO, and rGO. Graphene becomes p-type naturally, when it interacts with adsorbates like oxygen or water molecules. Graphene doped with n-type does not occur naturally. Doping graphene with n-type dopant is not very common. However, n-type doping of graphene can be produced by adding conducting polymers such as polyaniline (PANI) or polyurethane acrylate (PUA) or $N11_3$ gas. The covalent bond between nitrogen atoms and carbon atoms of graphene or noncovalent interaction of polymers and graphene forms n-type graphene. Graphene doped with polymers enhances mobility of carriers due to the presence of low disorder and charge neutral states [9].

In this chapter, polyethylenimine (PEI) polymer has been used as the dopant for doping graphene derivatives, GO, and rGO. PEI is a water soluble polymer. It consists of amine groups. Each amine has a nitrogen atom with a lone pair. It can donate electron through charge transfer to form n-type GO and rGO. The effect of doping GO and rGO with PEI have been investigated thoroughly and compared with =doped GO and rGO. Nanocomposites of PEI doped GO and rGO have been prepared by drying

solution of PEI/GO and PEI/rGO in deionized water. PEI doped GO and rGO have been deposited using the electrochemical deposition (ECD) technique on a glass substrate coated with indium tin oxide (ITO). The prepared nanocomposites and thin films have been characterized by using different techniques including cyclic voltammetry (CV), electrochemical impedance spectroscopy (EIS), scanning electron microscopy (SEM), FTIR, CHN analysis, Raman spectroscopy, and XRD tests.

10.2 EXPERIMENTAL METHODOLOGY

10.2.1 MATERIALS AND CHEMICALS

PEI, MW—5000 and potassium hydroxide (KOH) were purchased from Sigma-Aldrich. GO and rGO powder were prepared as discussed in the next section. ITO coated glass (15 Ω /sq) was purchased from NANOCS. Distilled water, or DI water, was used to prepare each solution.

10.2.2 PREPARATION OF GO AND RGO

GO has been synthesized as discussed in details in Ref. [10]. Chemical oxidation method has been used instead of using the Hummers method. It involves a two-step method. In the first step, HNO_3 (nitric acid) and H_2SO_4 (sulphuric acid) were used to oxidize the graphite flakes. Then, $KMnO_4$ was used for further oxidization to synthesize GO. It is a modified Hummer method for GO synthesis. This method produces a large volume of GO.

GO is a chemical that has garnered a lot of interest in recent years for its unique characteristics and prospective applications. It is a two-dimensional honeycomb lattice made up of atoms of carbon, oxygen, and hydrogen stacked together in a single atomic manner. Through a sequence of oxidation and exfoliation procedures, graphite, the same substance used in pencil lead is converted into GO. It has potential for many different

applications because of these qualities, which include energy storage, sensors, biomedical applications, and so forth.

GO is commonly reduced via chemical, thermal, or electrochemical techniques to eliminate these oxygen-containing groups, yielding a material with characteristics closer to pristine graphene. rGO retains graphene's unique features, such as strong electrical conductivity, superior mechanical strength, and vast surface area, making it appealing for a wide range of applications, including energy storage devices, sensors, catalysis, and composites. The reduction procedure can also restore graphene's π-conjugated structure, which increases its electrical conductivity compared to GO. rGO is a substance formed by reducing GO and removing oxygen-containing functional groups from it. GO is a derivative of graphene, which is a single layer of carbon atoms organized hexagonally [37].

rGO has been synthesized from Citrus grandis (Pomelo) phytochemical extracts using a green method as reported in Ref. [4]. GO was reduced using this environmentally friendly method. White Pomelo juice with antioxidant property was extracted using juicer and reduced to GO. This is a low cost method that does not produce any hazardous byproducts. It only produces water and organic compounds as byproducts. Mass production of rGO is possible without causing any harm to the environment.

10.2.3 DOPING OF GO AND RGO

PEI, an amine rich conducting polymer is used for doping and functionalization of GO and rGO. PEI is an organic polyamine polymer with repeating unit composed of the amine group. Figure 10.4 shows the structure of PEI. All PEI polymers are hydrophilic and may contain approx. 30% hydrated water. It is freely miscible with water at room temperature. PEI is an electron-donating polymer with a high amine content. The nitrogen atom of PEI has a lone pair of electrons available for donation.

Hence, it is an n-type dopant. PEI doping may donate its extra valence electrons to the conduction band of a semiconductor material, increasing the concentration of CNTs electron. The Fermi level of the semiconductor might move toward the conduction band due to doping. It has one nitrogen with a lone pair in every three atoms in the amine structure. The nitrogen atoms donate electron to GO and rGO [11]. Consequently, this changes the electrical conductivity and dispersibility due to functionalization. GO contains a large amount of oxygen containing groups (e.g., −OH, −C = O, −COOH). Adding PEI to GO partially reduces it [12]. It is an environmentally friendly reduction technique. PEI interacts with GO and rGO by covalent bonds and/or electrostatic interactions. The −COOH groups present at the edges of GO are replaced by NH_2 of polymer PEI for covalent modification [13]. GO contains π-network, which are disruptive. Reductive treatment of GO removes functional groups and partially recovers sp^2 hybridization, the aromaticity [14]. Ten milliliters of ethanol was mixed with 5 mg of the synthesized GO powder. For 20 min, the solution was sonicated. Next, it was mixed with 2 mg of PEI. To create a homogenous solution, the liquid was sonicated for 30 min and agitated for 15 min It was kept for 24 h at room temperature and then for 12 h at 40°C in a vacuum oven to form PEI doped GO powder. Similarly, the synthesized rGO powder, 5 mg was added to 10 mL of ethanol. The solution was sonicated for 20 min Then, 2 mg of PEI was added to it. The mixture was sonicated for 30 min and stirred for 15 min to form a homogeneous solution. It was stored at room temperature for 24 h and in a vacuum oven at 40°C for 12 h to form PEI doped rGO powder.

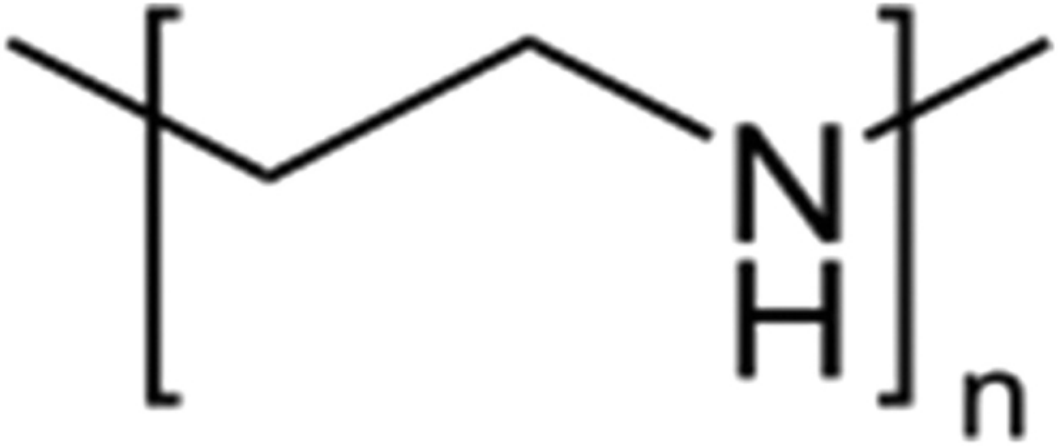

FIGURE 10.4 Structure of polyethyleneimine (PEI).

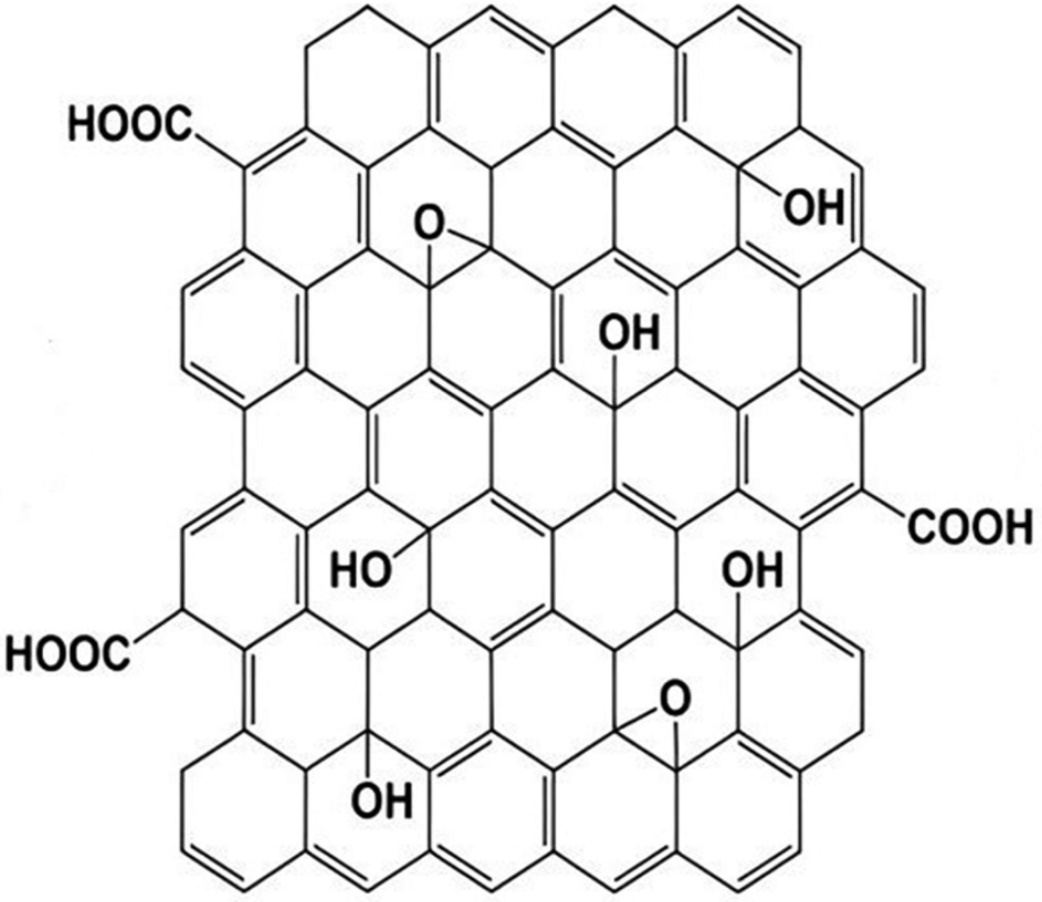

FIGURE 10.2 Structure of graphene oxide.
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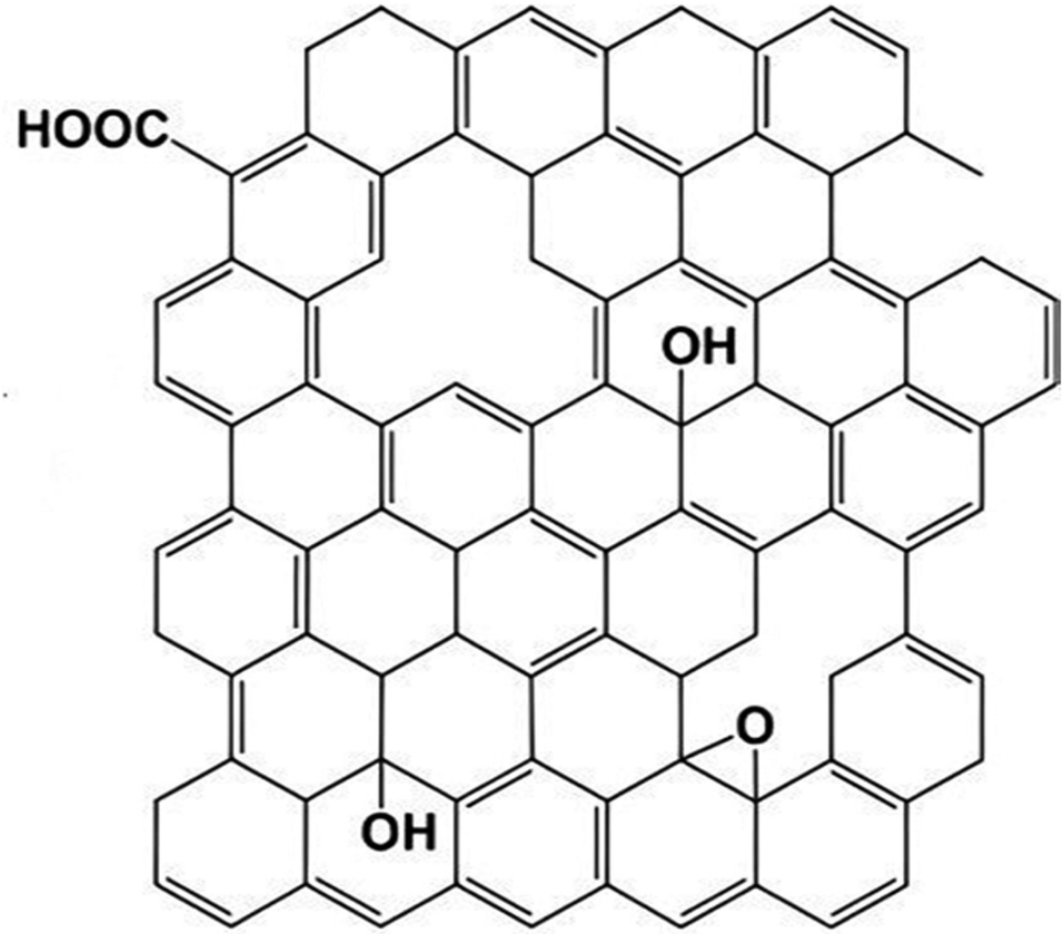

FIGURE 10.3 Structure of reduced graphene oxide.
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10.2.4 THIN FILM DEPOSITION

The synthesized GO and rGO, and PEI doped GO and PEI doped rGO have been deposited on an ITO glass (dimension–3 × 2 mm) for in-liquid measurements. ECD technique was used to deposit the different films from the prepared solutions. Autolab Potentiostsat/Galvanostat consisting of a three electrode electrochemical cell with ITO coated glass substrate as the working electrode, Pt wire as counter electrode, and Ag/AgC1 electrode as the reference electrode were used for deposition of the layers [11]. For deposition of GO layer, a solution of GO and ethanol was prepared by

dissolving 5 mg of GO in 10 mL of ethanol. The solution was sonicated for 30 min and stirred for 15 min by using ultrasonic probe sonicator and magnetic stirrer. It was then deposited on the ITO coated substrate. For deposition of rGO layer, a solution of rGO and ethanol was prepared by dissolving 5 mg of rGO in 10 mL of ethanol. To homogenize the solution, an ultrasonic probe sonicator and a magnetic stirrer were used for 30 min of sonication and 15 min of stirring. It was then deposited on the ITO coated substrate. For deposition of PEI doped GO layer, 5 mg of GO was dissolved in 10 mL of ethanol to create a GO and ethanol solution. In this solution, It was mixed in 2 mg of powdered PEI. Using a magnetic stirrer and ultrasonic probe sonicator, the solution was sonicated for 30 min and stirred for 15 min It was then deposited on the ITO coated substrate. For deposition of PEI doped rGO layer, a solution of reduced GO and ethanol was prepared by dissolving 5 mg of GO in 10 mL of ethanol. Two milligrams of powdered PEI was added to this solution. Using a magnetic stirrer REMI 1-MLH and an ultrasonic probe sonicator SONAPROS PR-1000 MP, the solution was sonicated for 30 min and stirred for 15 min. It was then deposited on the ITO coated substrate. Each of the film was then heated at room temperature for 24 h and in a vacuum oven at 40°C for 6 h. Then using the gravimetric analysis method, the thickness of each layer was determined and found to be around 100 nm [11]. Deposition of PEI doped GO and rGO on the ITO coated glass changes the visibility compared to the GO and rGO deposited film. Thus, polymer presence can be determined on the films [9].

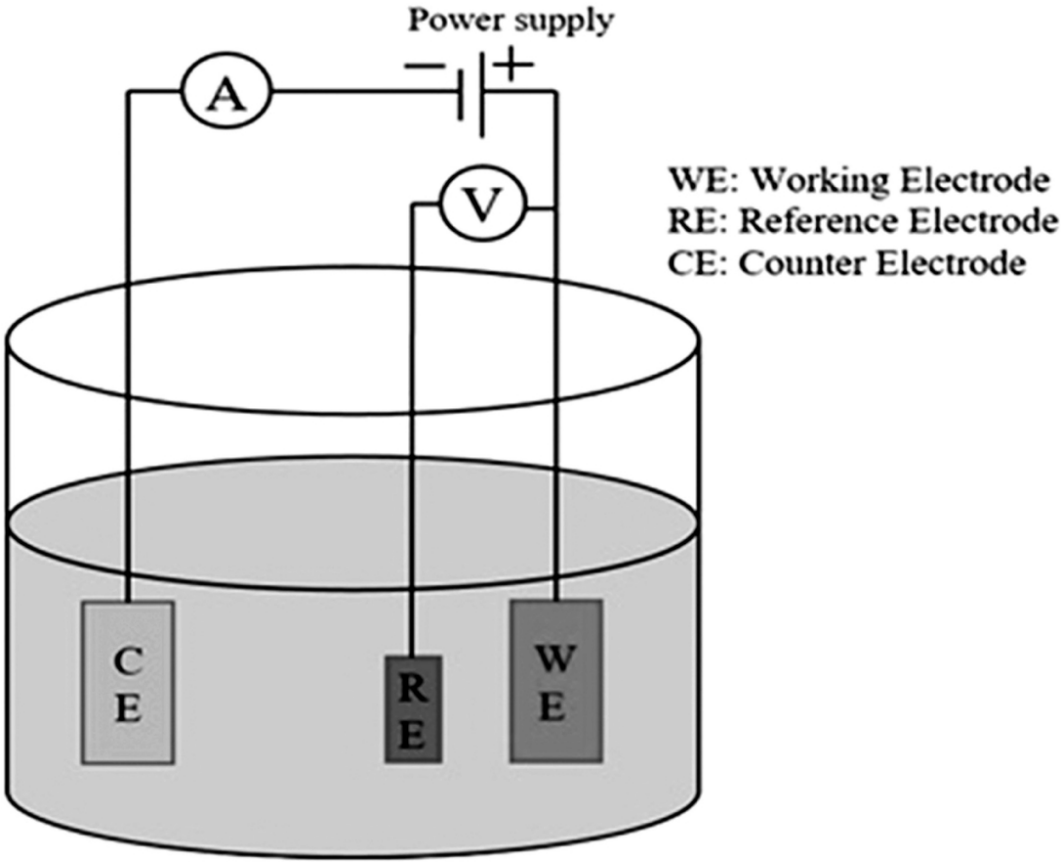

FIGURE 10.5 Electrochemical deposition system.

10.2.5 INSTRUMENTS UTILIZED FOR CHARACTERIZATION

X-ray diffraction (XRD) pattern was recorded by using the software XRD Commander 2 and Diffrac.EVA (Make: Bruker AXS, Germany, model no. D8 FOCUS). The FTIR spectrum the model Forntier IR (Make: Perkin Elmer). SEM images were studied to analyze the surface morphology using the model JSM 6390 LV (Make: Jeol, Japan) with Jeol Software, (Windows based). CV test was carried out by using Autolab Potentiostsat/Galvanostat, PGSTAT128N system having software Nova 2.1. Raman spectroscopy analysis was performed by using Raman spectrometer (Make: Renishaw, UK, model: Renishaw basis series with 514 Lasers, software: Wire 3.4). CHN analysis was performed by using CHN Analyzer (Make: Perkin

Elmer, USA, model: 2400 SERIES 2) to detect carbon (C), hydrogen (H), and nitrogen (N) elemental content in the prepared samples. UV-Vis spectroscopy analysis was carried out by using UV-Visible spectrometer (Make: Shimadzu, model: UV-2450, software: UV Probe 2.32) to study optical, absorption, reflection, and transmission through a sample.

10.3 RESULTS AND DISCUSSIONS

10.3.1 ELECTROCHEMICAL MEASUREMENT

These prepared samples were used for in-liquid measurement by CV tests. CV has been employed to study the interface barrier kinetics. Generally, the resistance to electron transfer increases with increase in thickness and tends to decrease with barrier defect density [15]. The prepared samples were inserted, one at a time in a glass containing a 3 M KOH electrolyte solution and the three electrodes. Figures 10.6(a) and 10.7(a) display the CV curves measured in the potential range of 0 V to 0.5 V at a scan rate of 100 mV/s. The CV is current response as a function of applied potential. The potential range is determined by the solvent, electrolyte, and the materials. The current of the working electrode is plotted versus the applied voltage. It is used to study the electrochemical properties of an analyte in solution. It measures the current that takes part in redox reactions. The obtained curve is symmetric. CV provides information on faradaic redox reactions. There is negligible distortion in the curve and it represents that the redox process is rapid and reversible [16]. The CV curves of GO and PEI doped GO are shown in Figure 10.6(a). It shows that the area of the PEI doped GO curve is lager compared to GO curve. The large integrated area under the curve of the PEI doped GO sample results in a larger capacitance value and hence larger charge storage capability. A large capacitance results in a larger sensitivity of biosensor and large charge storage capability for super

capacitors [4, 17]. PEI has large amount of primary and secondary amine groups. This group donates electrons to GO and changes the conductivity. It also partially reduces and functionalizes GO by eliminating the oxygen-containing functional groups. The lower integrated area under the curve of GO means the specific capacitance is lower compared to PEI doped GO. Figure 10.1(b) and (d) shows the Nyquist plot in the frequency range of 100 MHz to 100 KHz for EIS data of GO and PEI doped GO. The Nyquist plot depends on the composition of the working electrode as well as the electrochemical reactions taking place either at the working electrode surface or bulk of the solution. The solution resistance of GO and PEI doped GO are 97.5 and 540 n, respectively. The charge transfer resistance (R_{ct}) is lower in PEI doped GO compared to GO. This justifies the higher integrated area under the curve of the PEI doped GO as opposed to GO. W is known as Warburg impedance. It depends on frequency. This additional resistance is created by diffusion of molecules or redox species at the electrode-electrolyte interface. CPE is constant phase element (CPE) of double layer as a perfect capacitor does not exist. CPE is used to model the non-ideal capacitance behavior [18]. The Nyquist plot is semi-circular and partly linear for high frequency and low frequency data, respectively. The Randles equivalent circuit models of GO and PEI doped GO are shown in Figure 10.6(c) and (e), respectively. The series resistance (R_s) can be obtained from the intercept value of the real axis. It represents the electrolyte and electrode internal resistance. The R_{ct} is represented by the semicircle diameter along the real axis. The access of the electrolyte to the sample (thin films) is reflected by the low frequency linear region. As the pores in the sample become wider the slope increases and vice-versa.

FIGURE 10.1 Structure of graphene.

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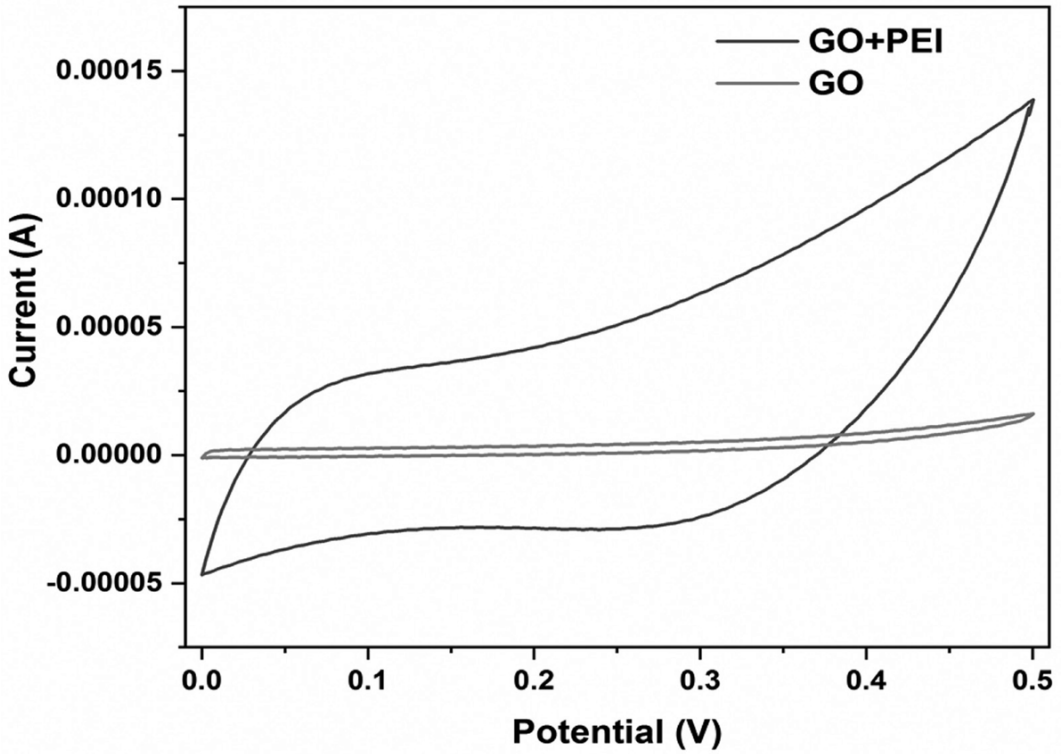

FIGURE 10.6A Cyclic voltammogram (CV) curves of GO and PEI doped GO.⏎

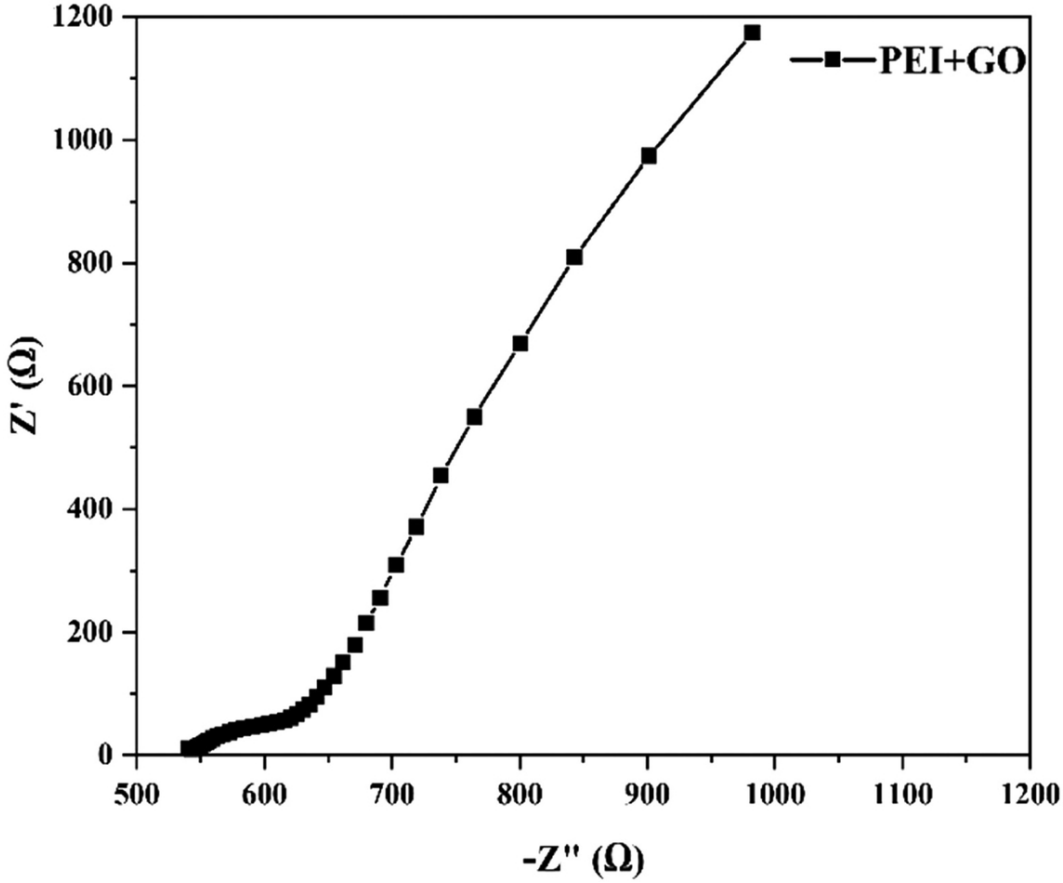

FIGURE 10.6C Electrical equivalent circuit for GO EIS data.

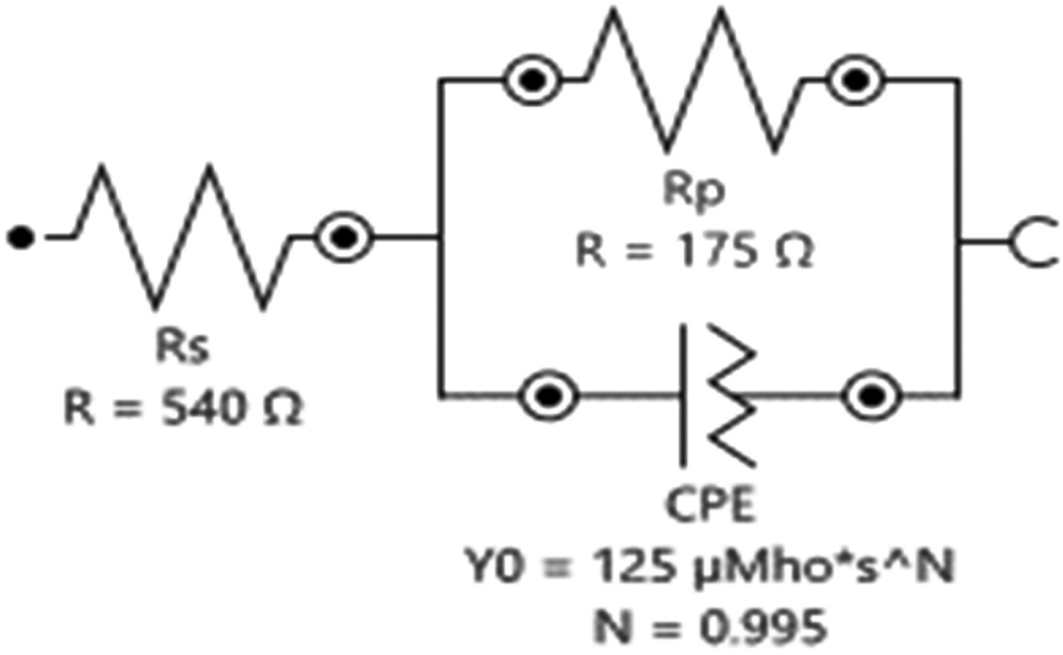

FIGURE 10.6E Electrical equivalent circuit for PEI doped GO EIS data.

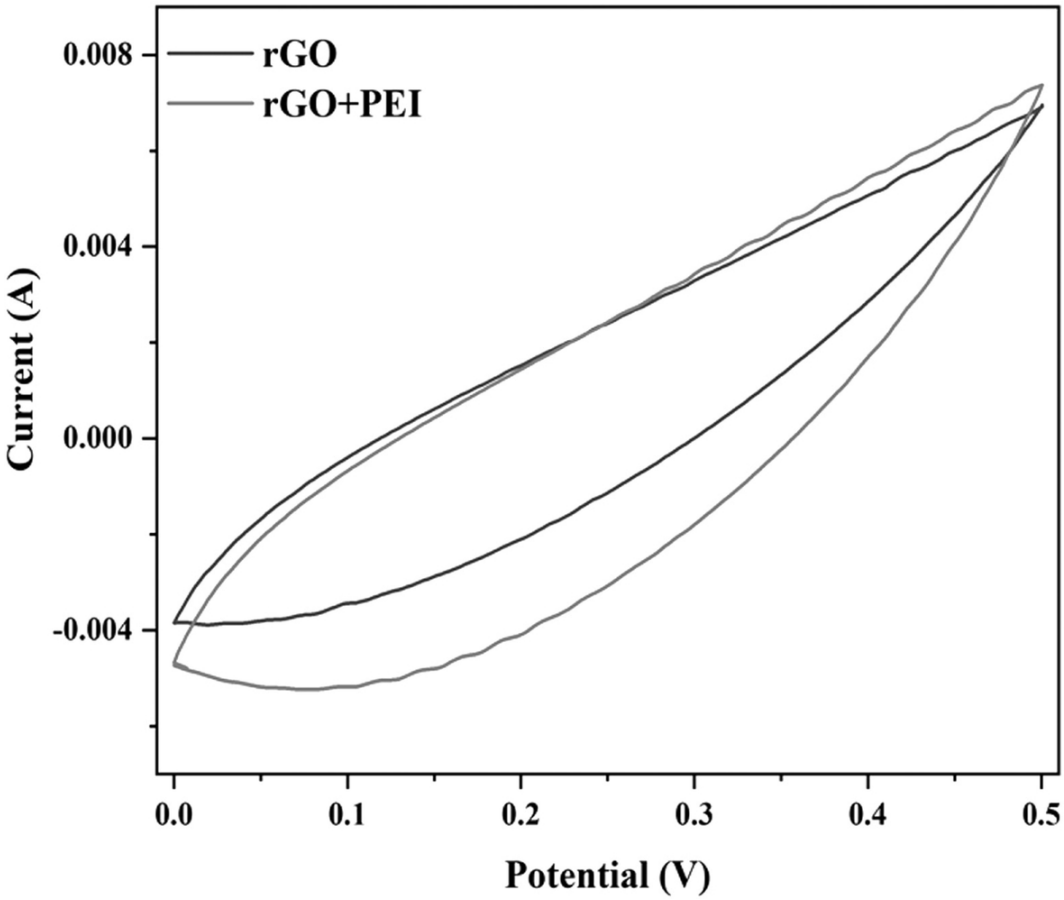

FIGURE 10.7A Cyclic voltammogram (CV) curves of rGO and PEI doped rGO.

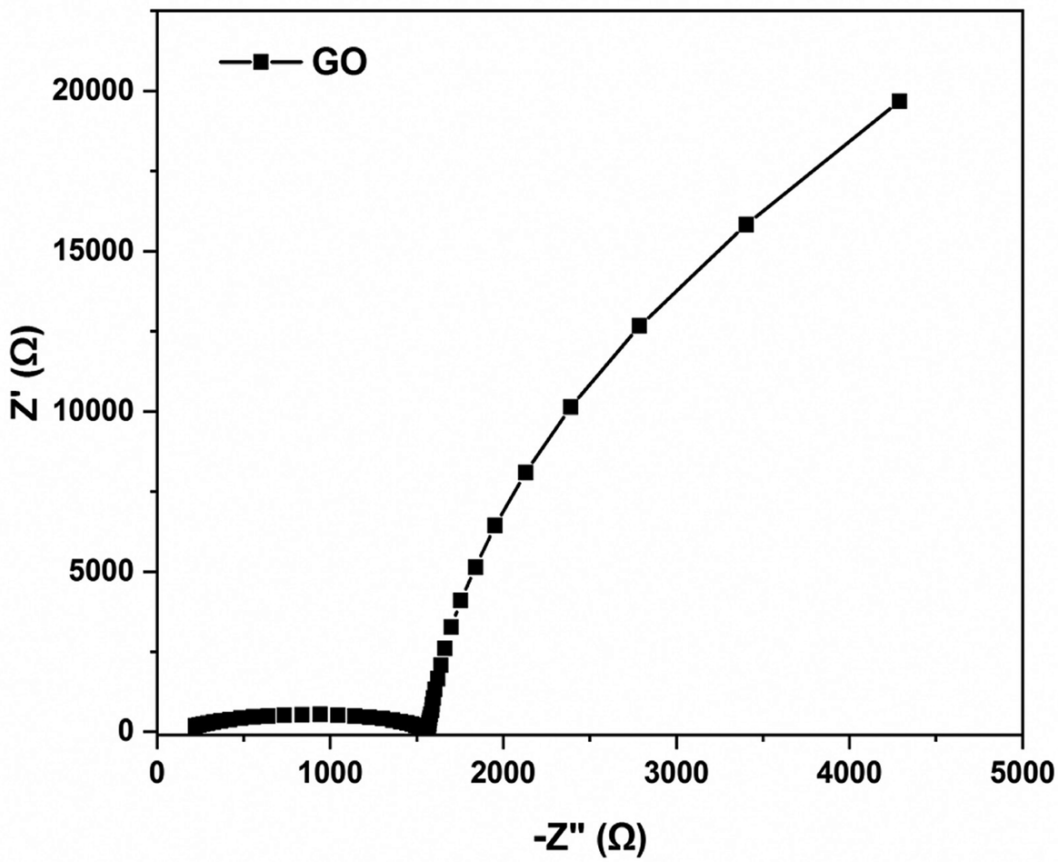

FIGURE 10.6B Nyquist plot of graphene oxide.

Figure 10.7(a) shows the CV curves of rGO and PEI doped rGO. The curves were recorded at a scan rate of 100 mV/s in the applied potential range of 0-0.5 V. The high symmetric nature of the curve demonstrates excellent capacitive behavior. The area of the PEI-rGO curve is larger compared to GO. PEI doping increases the conductivity of rGO and hence larger area has been obtained. This implies improved electron transfer between the electrode and electrolyte solution due to PEI doping in rGO. Consequently, more ions accumulate at the electrode surface. This has been justified by the Nyquist plot (Figure 10.7(b)) and the electrical equivalent circuit shown in Figure 10.7(c) and (d). The series resistance also changed due to addition of PEI in rGO. The Nyquist plot indicates PEI doping

improves electrical conductivity of rGO. The semicircle at high frequency of PEI doped rGO is more depressed compared to rGO.

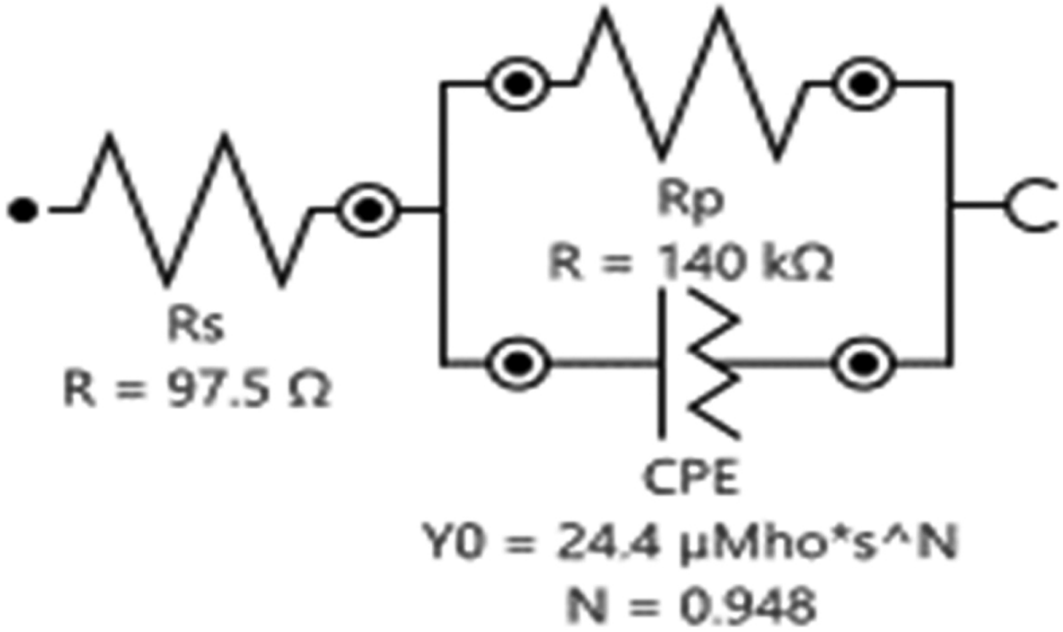

FIGURE 10.6D Nyquist plot of PEI doped GO.

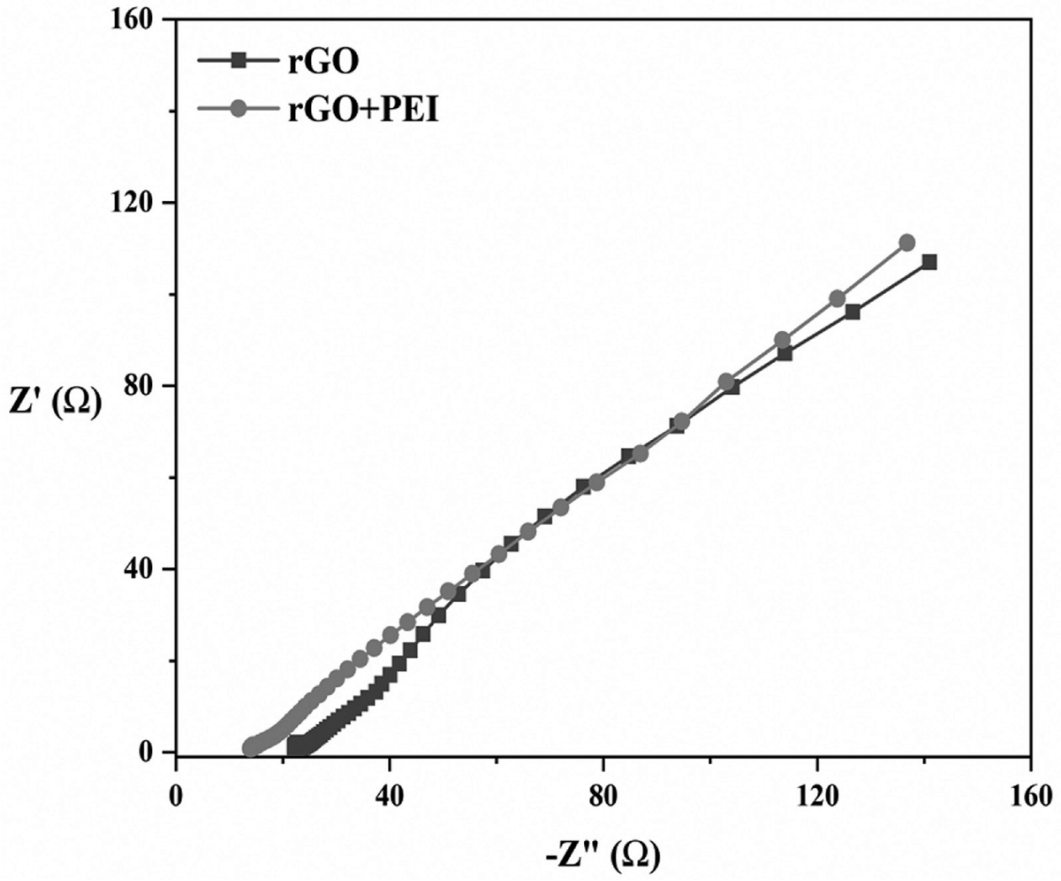

FIGURE 10.7B Nyquist plot of rGO and PEI doped rGO.

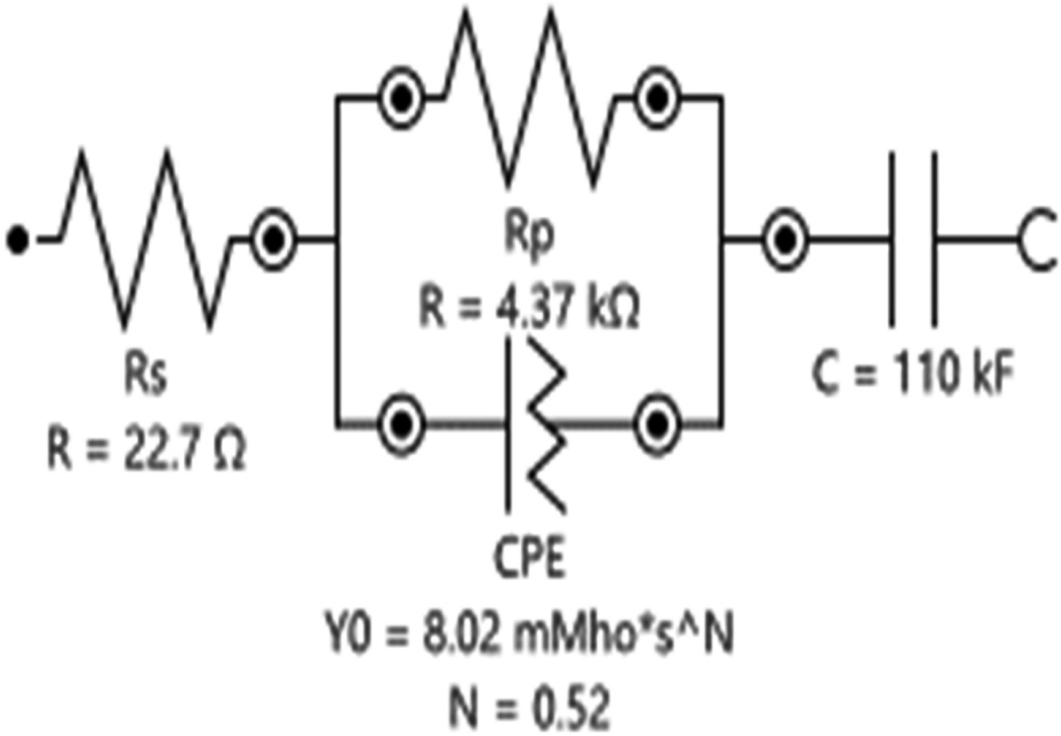

FIGURE 10.7C Electrical equivalent circuit for rGO EIS data.

The specific capacitance (C_s) in the unit of Fg^{-1} can be calculated from the curves by using the formula [4]:

$$C_s = \frac{1}{m * s * \Delta V} \int_{V_1}^{V_2} I(V)dV$$

where, m is mass of active materials, Δv is the potential window, s is the scan rate (V/s), I (V).dV is the integrated area under the curve and V is the applied potential.

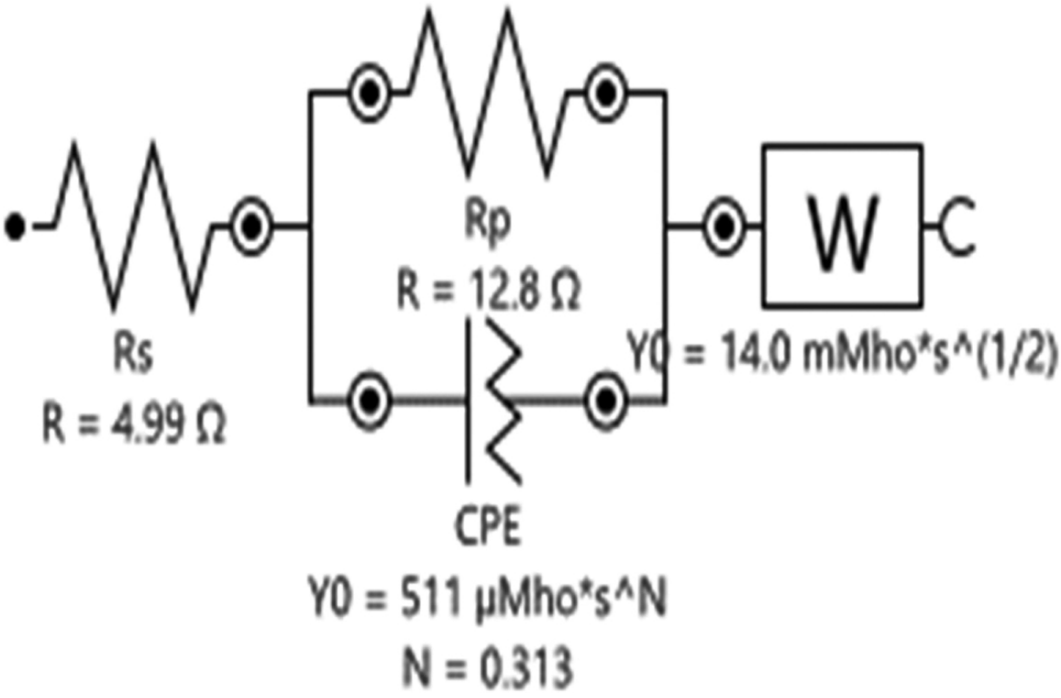

FIGURE 10.7D Electrical equivalent circuit for PEI doped rGO EIS data.

The area under the curves in Figures 10.6(a) and 10.7(a) are calculated for the samples GO, rGO, PEI doped GO, and PEI doped rGO. The mass of each of the samples was taken as 1 mg. The potential window is 0-0.5 V.

The scan rate is 100 mV/s. The specific capacitances were calculated as 3.2 × 10^{-2} F/g, 0.656 F/g, 26 F/g, and 40 F/g for GO, PEI doped GO, rGO, and PEI doped rGO, respectively. The PEI rGO has highest area and highest specific capacitance and hence conductivity is evident from the Nyquist plot and the electrical equivalent circuit.

10.3.2 FTIR SPECTROSCOPY

The prepared powder samples of GO, PEI doped GO, rGO, and PEI doped rGO were used for analysis using Fourier transform infrared spectroscopy (FTIR). This analysis gives information about chemical composition, structural modifications, and interaction between different molecule. This technique is used for functional groups identification within molecules. These groups vibrate through mechanisms, such as stretching or bending depending on the wavelengths of light used for irradiation. Thus, this technique examines molecular vibrations.

The FTIR spectrum was recorded in the range of 500–4000 cm^{-1}. Figure 10.8 shows the spectral comparison of GO, PEI doped GO, rGO, This confirms the presence of PEI in the PEI doped GO [12, 18]. The strength of the broad peak observed in the range of 3000–3600 cm^{-1} in PEI-GO decreases. It is due to the addition of amine group ($-NH_2$) in place of hydroxyl group. and PEI doped rGO. It can be seen that there are significant spectral differences. The broad peak observed in the range of 3000-3600 cm^{-1} in GO is attributed to hydroxyl group. It is due to O-H stretching. The hydroxyl group is formed due the −COOH group and H_2O. The other observed peaks at 1079, 1364, 1624, and 1736 cm^{-1} are due to C−O stretching, the O−H deformation vibration, the skeletal vibration of un-oxidized graphitic domain, and C = O stretching vibration in carboxyl acid (or carbonyl group), respectively [12, 19, 20 and 21]. Due to addition of PEI in GO, some new peaks are seen at 748, 1135, 1267, 1563, 2880, and

2945 cm^{-1}. The peaks corresponding to 748 and 1135 cm^{1} are due to C−H and C−N stretch, respectively [12]. The peak at 1736 cm' disappeared due to PEI addition to GO from GO spectra. The strength of the peaks at 1624 cm^{-1} increases. Peaks at 1267 and 1563 cm^{-1} are due to the vibrations of C−N stretching and N−H bending. This confirms the chemical reaction between PEI and GO [18]. The observed peaks at 2880 and 2945 cm^{-1} represent the CH_2 stretching modes of PEI, which are symmetric and asymmetric.

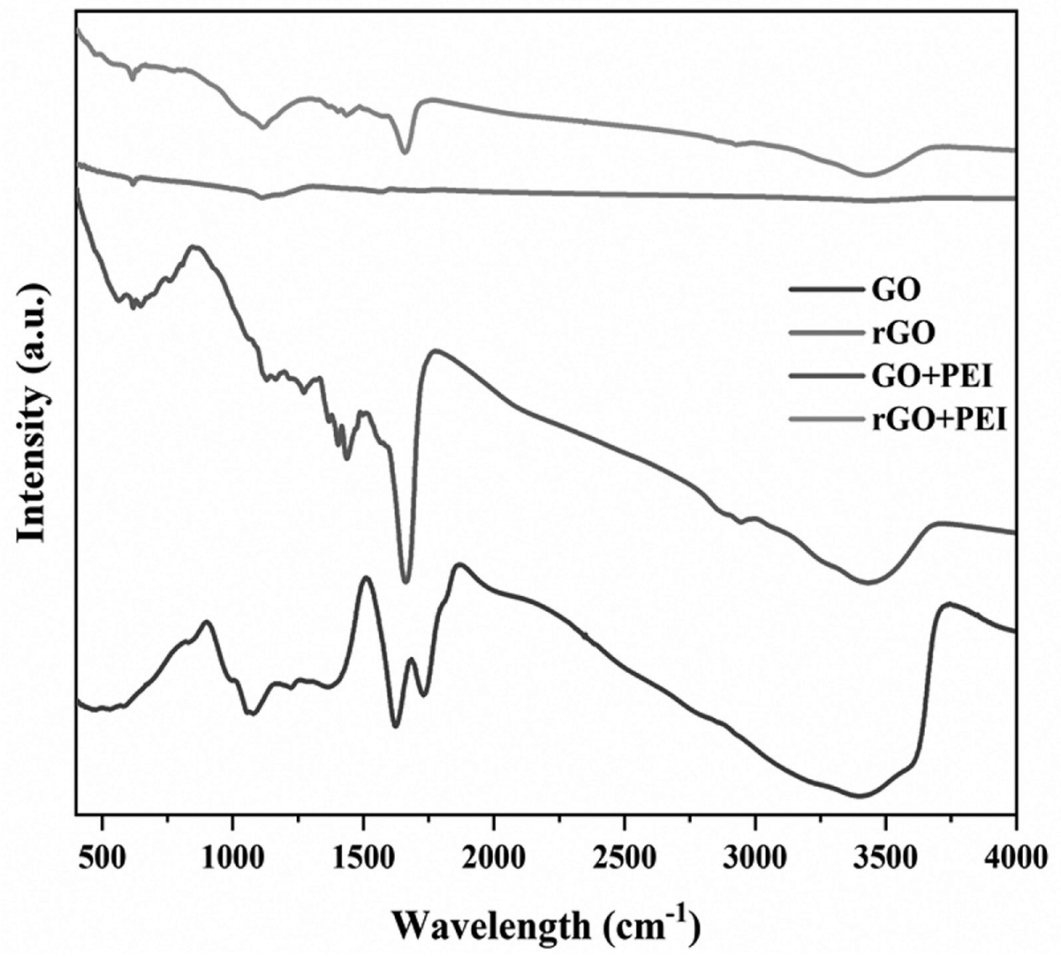

FIGURE 10.8 FTIR spectra of GO, rGO, PEI doped GO, and PEI doped rGO.

The peak intensities decrease in rGO except at 1624 cm^{-1}. This may be attributed to the reduction of oxygen containing functional groups such as carboxyl, hydroxyl, epoxy, and carbonyl of GO and the formation of rGO [18]. In PEI doped rGO, the strength of the peaks further decreases due to further reduction of oxygen containing functional groups. This confirms the bonding of PEI with rGO. These peaks resemble the PEI peaks. The several peaks observed around 1114, 1438, 1584, 1656, and 2947 cm^{-1} ascribed to C−O stretch, NH stretch, O−H bending of carboxylic acid, N−H bending vibration of primary amine, C−H, and N−H stretch, respectively. The peak at 1656 cm^{-1} is due to N−H bending vibrations in PEI. This indicates that PEI doped rGO is covalently modified by PEI [20, 22, 23]. The strength of the broad peak around 3500 cm^{-1} due to PEI doping rGO decreases. The PEI doping further reduces rGO.

10.3.3 XRD ANALYSIS

XRD pattern has been used to analyze the crystalline nature of GO, PEI doped GO, rGO, and PEI doped rGO. It was performed at a wavelength of 0.1540598 nm. Figure 10.9 shows the XRD patterns. There is an intense and sharp peak around 11.3°, which represents (002) plane. This corresponds to an interlayer spacing of 0.783 nm. It confirms the formation of GO layer with oxygen containing functional groups [24, 25]. This further means the spacing between the inter-layer GO sheets increases due to addition of oxygen containing functional groups [26]. This intense and sharp peak disappeared after PEI doping in GO, which means PEI has been successfully added to GO. This justifies that the diffraction pattern disappears or becomes weaker due to addition of PEI. However, there is a board peak around 21°. This corresponds to an interlayer spacing of 0.423 nm. The interlayer spacing between graphene sheets reduces due to the removal of the oxygen containing functional groups. There is a broad peak

around 23.6° for rGO corresponding to the (002) plane. This corresponds to an interlayer spacing of 0.377 nm [27]. This is due to the removal of oxygen containing functional groups. This indicates that the interlayer spacing between graphene sheets decreases [25]. The graphene layers restack again and move closer to graphitic structure [28]. In PEI doped rGO, the broad peak shifted to 24.5°. This shift is due to addition of PEI to rGO. This corresponds to an interlayer spacing of 0.363 nm. [20, 21]. Thus, the graphitic structure is restored again. The GO and rGO match the JCPDS 75-1621 and JCPDS 75-2078, respectively.

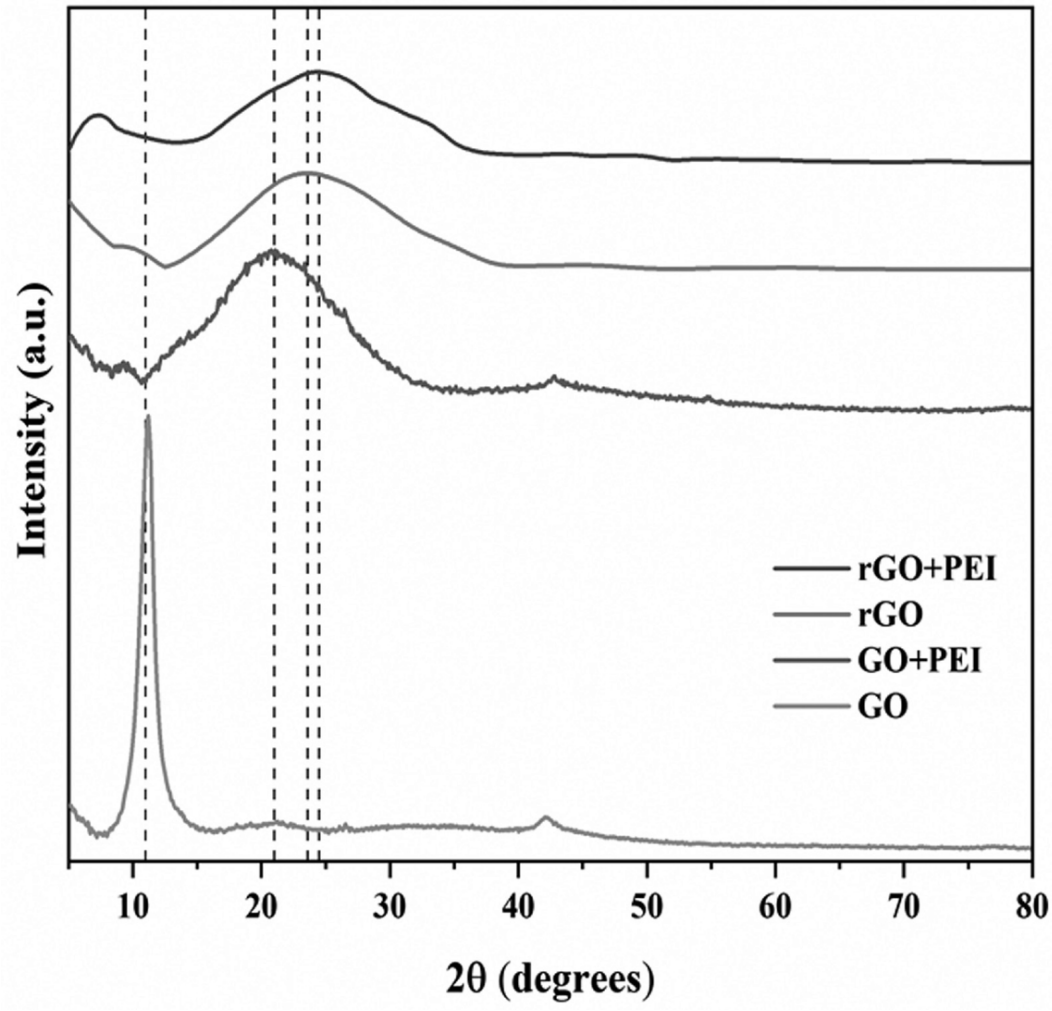

FIGURE 10.9 X-ray diffraction pattern of GO, rGO, PEI doped GO, and PEI doped rGO.

10.3.4 RAMAN SPECTROSCOPY

Raman spectroscopy analysis, a non-destructive technique was carried out to investigate the crystallographic structure of the prepared powder samples —GO, PEI doped GO, rGO, and PEI doped rGO. It was performed by using 514 nm wavelength lasers. The characteristic D and G peaks of the GO sample are present at 1345 and 1600 cm^{-}‘, respectively as shown in Figure 10.10. The peaks are sharp and have narrow widths. The D band at 1345 cm^{-1} is due to disorder, defects, and disruption in the graphitic domain. The G band is due to the in-plane sp^2 hybridized carbon atoms vibrations. The ratio of the intensity of D peak to the intensity of G peak (I_D/I_G) shows the amount of defects present in the sample under investigation [29, 30 and 31]. For GO, the ratio was found to be 0.89. The sharp peak intensity reduces in PEI doped GO and the widths of the peaks become broader. The peaks appeared at lower wavenumber. The I_D/I_G ratio was found to be 1.008. This value is higher than that of GO. This increase in the ratio confirms that there is interaction between PEI and GO, which partially reduces GO [32]. It means the average sizes of sp^2 domains decrease. For rGO, the I_D/I_G ratio was calculated as 0.983. The widths of peaks are broader and peak intensity reduces compared to GO. This indicates the removal of the oxygen containing functional groups from GO and formation of rGO. The spa carbon in GO becomes sp^2 carbon in rGO [33]. After PEI doping in rGO, the I_D/I_G ratio was calculated as 1.004. The widths of peaks are broader and peak intensity reduces compared to rGO. Addition of PEI increases defects or disorder of the samples and consequently the peaks shift to lower wavenumber. The higher I_D/I_G ratios in PEI doped GO and PEI doped rGO might be due to the addition of polymers on the graphene sheets [34].

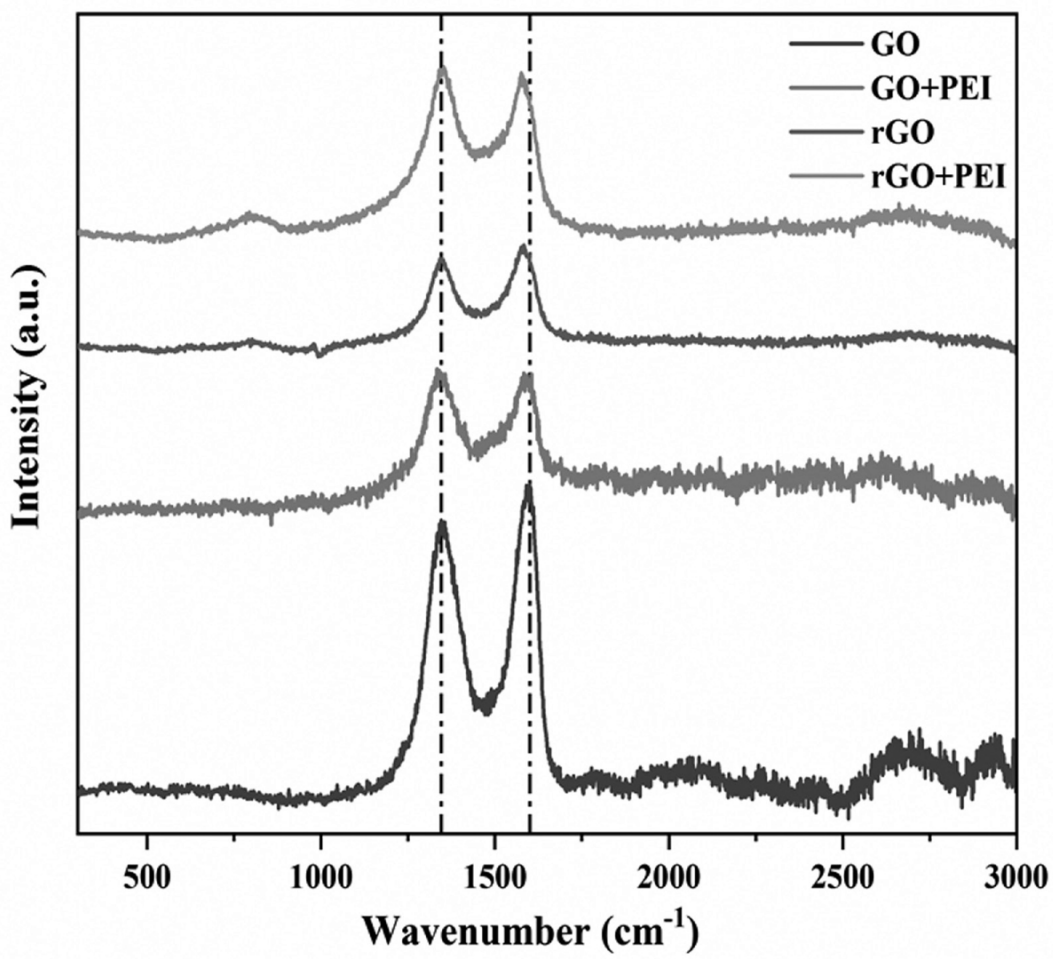

FIGURE 10.10 Raman spectra of GO, rGO, PEI doped GO, and PEI doped rGO.

10.3.5 SEM ANALYSIS

The deposited films on ITO coated glass substrate were imaged by SEM. The SEM image shows the morphology of the deposited films. The SEM image of GO is shown in Figure 10.11(a). The surface is smooth and tightly packed. The deformation of the graphene sheet is less, though it shows the presence of agglomeration. In the graphene sheets, distinguishable edges and wrinkles are present [35]. However, there is a large amount of wrinkles and agglomeration in the PEI doped GO sheet. It is shown in Figure 10.11(b). The structure is porous with lot of adsorption sites in it. PEI addition to GO partly reduces it and deforms the sheet.

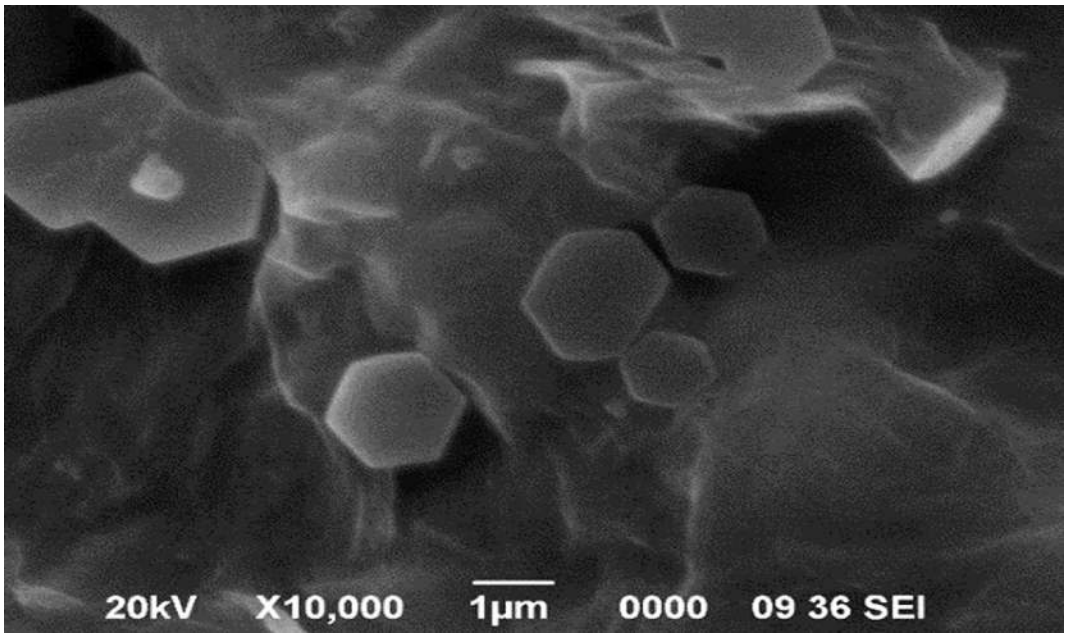

FIGURE 10.11A SEM micrograph of GO.

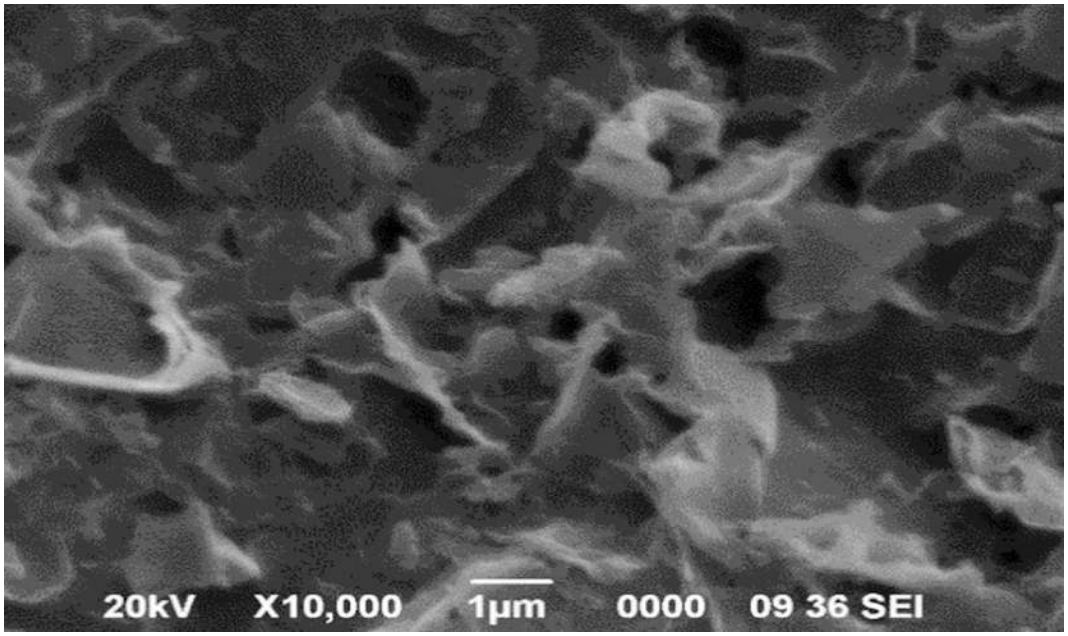

FIGURE 10.11B SEM micrograph of PEI doped GO.

Figure 10.11(c) shows the SEM image of rGO. Due to reduction of GO, many wrinkles, distinct edges, and agglomeration occur in rGO [25]. The SEM image of PEI doped rGO is shown in Figure 10.11(d). Interaction of PEI with rGO further decreases agglomeration and reduces the free energy.

The rGO film crumples as a result of the formation of hydrogen bond between PEI amine groups and oxygen. The PEI doped rGO becomes closer to graphitic structure. The layered structure shows the sheets that are irregularly arranged.

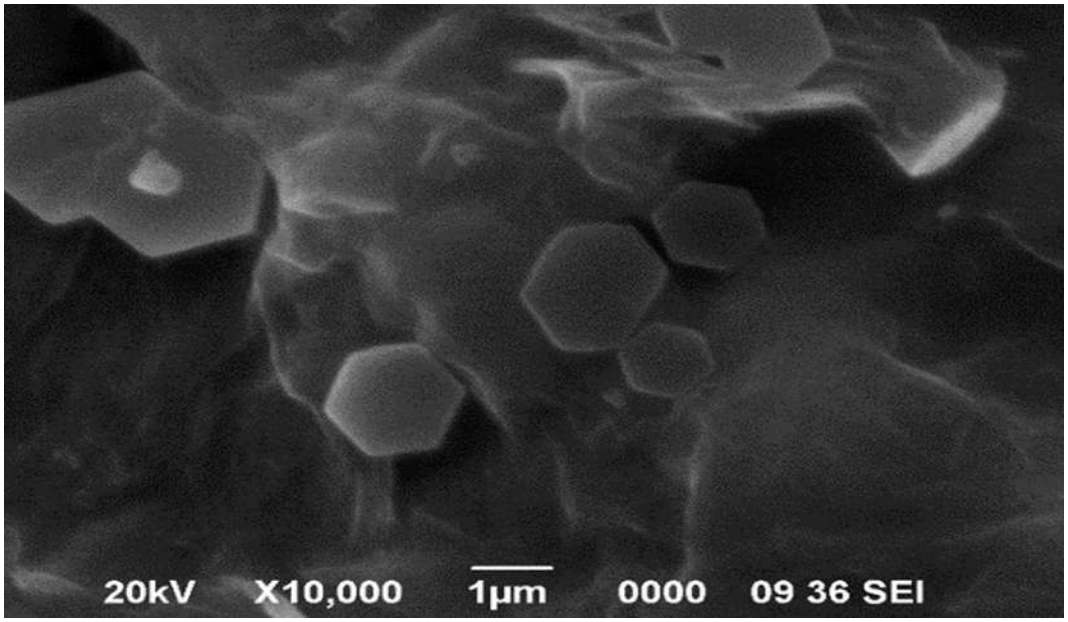

FIGURE 10.11C SEM micrograph of rGO.

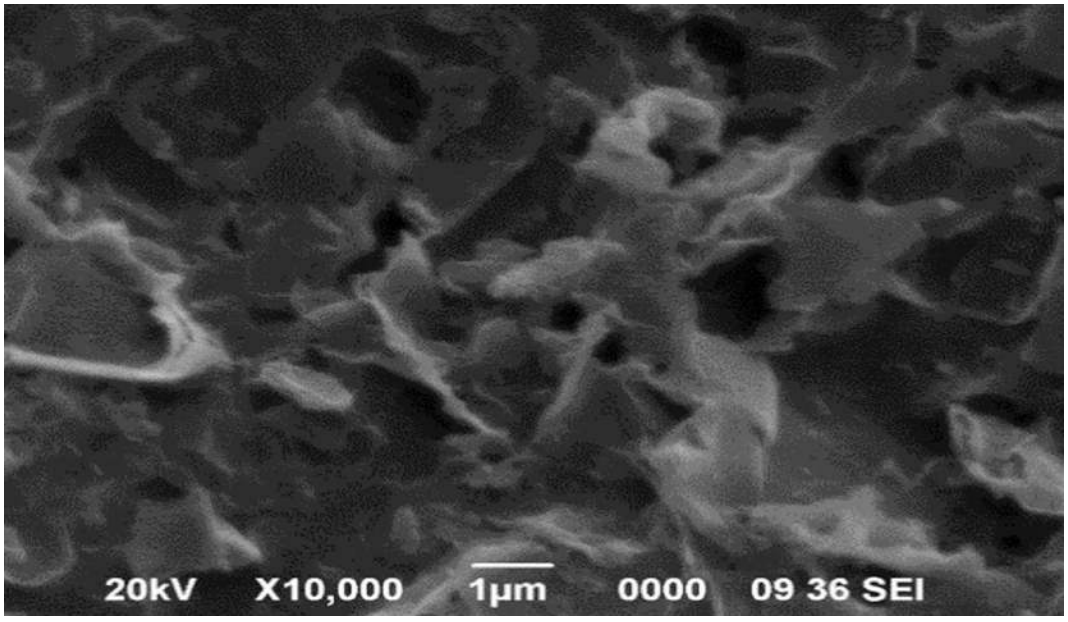

FIGURE 10.11D SEM micrograph of PEI doped rGO.

10.3.6 ELEMENT ANALYSIS

The content of different elements such as carbon (C), hydrogen (H), and nitrogen (N) in GO, PEI doped GO, rGO, and PEI doped rGO has been analyzed by using CHN elemental analyzer. Table 10.1 shows the CHN elements present in each of the prepared sample in percentage of mass. It gives information about the distribution of nitrogen in the samples. The carbon (C) content in the GO sample is lowest compared to other samples [36]. It increases in PEI doped GO due to partial reduction by PEI, whereas it is almost same in rGO and PEI doped rGO. The hydrogen content in PEI doped samples of GO and rGO is higher compared to GO and rGO. It is because of the amine group ($-NH_2$) present in PEI. There is no nitrogen element in GO and rGO. The nitrogen content becomes a significant percentage after doping GO and rGO with PEI, as it is rich in nitrogen element. This further confirms the doping of GO and rGO by PEI and formation of bonding between the two. The samples again get back the graphitic structure due to reduction oxygen containing functional groups. The increase in nitrogen (N) content in PEI doped rGO means more number electrons will be transferred to graphene layers, increasing the conductivity of the composite. This is in accordance with the CV results.

TABLE 10.1 CHN Elemental Analysis of Prepared Samples. ⏎

Sample	C (%)	H (%)	N (%)
GO	42.87	3.34	0
PEI-GO	47.79	7.37	18.31
rGO	50.77	1.15	0
PEI-rGO	50.60	4	10.64

10.4 CONCLUSION

In this chapter, GO and rGO have been doped with conducting polymer PEI by using solution process. Consequently, the conductivity of the GO and

rGO enhanced, as observed from electrochemical measurement, CV experiment. The intrinsic and interface resistance of the oxide layer and electrolyte reduces with increasing PEI doping concentration. The CHN analysis revealed that the PEI doped rGO contained a higher concentration of nitrogen species than the other samples. This enhances the conductivity of rGO due to the available lone pair electrons of nitrogen in the amine group of PEI. The CV analysis of PEI doped rGO demonstrated the high surface area and high specific capacitance of 40 F/g at a scan rate of 100 mV/s. In addition, the EIS analysis of PEI doped rGO showed the lowest equivalent series resistance (—5 Ω) and R_{ct} (12.8 Ω) due to the PEI doping. The experimental results show that n-type graphene can be synthesized by using PEI as dopant to improve graphene based biosensors performance. These research findings will help researchers to understand and utilize polymers to different biosensors based on nano-material graphene.

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KEYWORDS

- **cyclic voltammetry**
- **electrochemical impedance spectroscopy**
- **GO**
- **graphene**
- **n-type graphene**
- **PEI doped GO**
- **PEI doped rGO**

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CHAPTER 11

A Numerical Approach to Investigate the Effect of Work Function on the Important Cell Parameters of Heterojunction Solar Cell

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ABSTRACT

$ZnO\text{-}SnO_2$ nanocomposite has garnered the attention of the researchers and the scientific community due to its applications in various optoelectronic devices. In this chapter, the potential application of $ZnO\text{-}SnO_2$ in heterojunction solar cell has been explored. The effect of bulk properties of the active semiconducting material on the important properties of the cell, including power conversion efficiency (PCE), open circuit voltage (V_{oc}), and short circuit current density (J_{sc}) was studied thoroughly with special focus on material work function (WF) since WF tuning significantly affects semiconductor device performance due to the creation of potential barriers

at the junction interfaces. It is observed that for the variation of WF from 4.6 to 4.0 eV, the J_{sc} insignificantly increased from 0.59 to 32.65 mA/cm^2, whereas the V_{oc} significantly enhanced from 0.62 to 0.65 V, resulting in the enhancement of the PCE of the cells from 4.43 to 17.56%. The present study can be very beneficial for the solar photovoltaic market.

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11.1 INTRODUCTION

ZnO and its composite nanostructure is an important emerging candidate in many electronic and optoelectronic devices, such as sensors [1, 2, 3 and 4], photocatalyst [5], thin film transistors [6], photodetectors [7, 8], super-capacitors [9], and heterojunction solar cells (HJSCs) [10, 11, 12 and 13] due to which it has garnered the attention of the researchers and the scientific community. The binary or the coupled semiconductor nanostructures are more advantageous than the pristine semiconductor due to having better electronic and optoelectronic properties, such as enhanced conductivity, carrier concentration, mobility, and reduced recombination.

In this direction, we explored the potential application of the ZnO-SnO_2 in the HJSCs by practically fabricating Au/ZnO-SnO_2/P-Si/Au HJSCs but, we could achieve a merely low conversion efficiency of just 3.98%. So, to explore the bottlenecks resulting to low power conversion efficiency (PCE), the effect of bulk electronic and optoelectronic properties of the active material on important cell parameters including J_{sc}, V_{oc}, and PCE has been investigated in this chapter. The key emphasis of this chapter is to investigate the effect of the material work function (WF) on the performance of the HJSCs.

11.2 MODELING AND SIMULATION

The structure of the HJSC depicting different layers under consideration for numerical simulation is depicted in Figure 11.1. The layers comprise back Au electrode deposited on the silicon substrate, spin coated ZnO-SnO_2 nanocompopsite, and the thermal metalized grid structure Au electrode. The transmittance ($Trans_{zs}$) was measured using UV—Visible spectroscopy and absorbance a(λ)of the sample under consideration and found to be almost 90%. The Taucs plot was used to calculate the bandgap and found to be 3.26 eV. The electronic and optoelectronic properties, such as conductivity, mobility, carrier concentration of the prepared samples were measured by hall measurement experiment. The WF of ZnO-SnO_2 is tunable in the range from 4.16 to 4.64 eV [14].

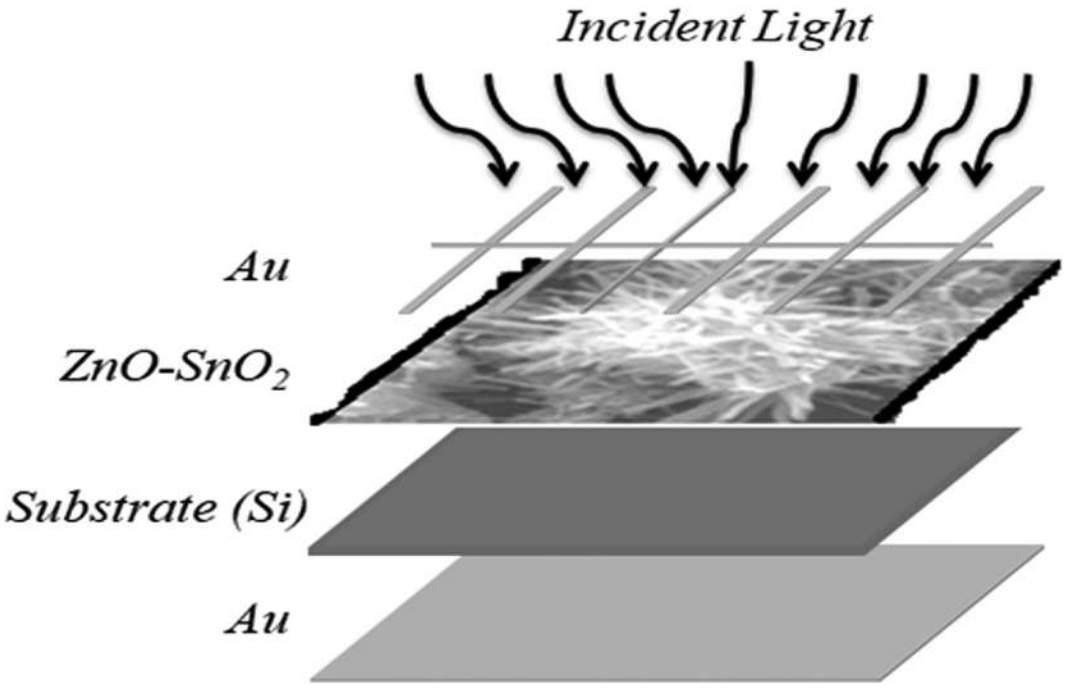

FIGURE 11.1 Device structure considered for simulation.

When light is illuminated upon the solar cells, it generates charge carriers due to photo excitation in both the space charge region and outside of the depletion region. Most of the photo excited carriers outside the depletion

region get recombined before being transported, having insignificant effect on the performance of the cells. Considering only the short waves, responsible for the photoexcitation in the depletion region, the expression for the depletion current ($J_D(\lambda)$) is equated in the Equation 11.1.

$$J_D(\lambda) = qTrans_{zs}(\lambda)\phi_{zs}(\lambda)\left[1 - e^{-\alpha(\lambda)W}\right] \tag{11.1}$$

where, q is electron charge, Trans (λ) is transmittance of ZnO-SnO_2, $\phi(\lambda)$ is WF, α(λ) is absorption coefficient, W is width of depletion layer given as:

$$W = \left\{ \frac{2\varepsilon}{qN_D}\left[(\phi_{zs} - \chi) - \frac{kT\ln(N_C/N_D)}{q} - \frac{kT}{q}\right]\right\}^{1/2} \tag{11.2}$$

The spectrum of the wave length in the range from 300 to 1100 nm is considered for simulation. So, the total photocurrent is obtained by integrating over this wavelength

$$J_{ph} = \int_{\lambda_1}^{\lambda_2} [J_D(\lambda)] \tag{11.3}$$

The expression for dark current is given as:

$$J_{\text{dark}} = J_o\left(e^{\frac{q(V-IR_s)}{nkT}} - 1\right) \tag{11.4}$$

where, J_0 is the dark saturation current and given by:

$$J_0 = qN_v e^{-\varphi_B/V_{th}} V_R \tag{11.5}$$

where, N_v is the effective density of the states, V_R is the mean unidirectional velocity, ϕ_B is the barrier height, expressed as:

$$\phi_{\mathrm{B}} = \mathrm{E_g} + \chi - \phi_{\mathrm{zs}} \tag{11.6}$$

where, E_{g}, χ, and ϕ_{zs} are bandgap, electron affinity, and WF, respectively.

The total photo current is the difference between the light generated current (I_{ph}) and the dark current (I_{dark})

$$\mathrm{I_{total}} = \mathrm{I_{ph}} + \mathrm{I_{dark}} \tag{11.7}$$

The open circuit voltage (V_{oc}), and photo-conversion efficiency are expressed as:

$$V_{oc} = V_{th} \ln\left[\frac{I_{ph} + I_o}{I_o}\right] \tag{11.8}$$

$$PCE = \frac{I_{\max} \cdot V_{\max}}{P_{in}} \tag{11.9}$$

where, $I_{\max}$, $V_{\max}$, and P_{in} (100 mn/cm^2) are maximum current, maximum voltage, and incident power, respectively.

11.3 RESULTS AND DISCUSSION

The short circuit current density enhanced slightly from 0.59 to 32.65 mA/cm^2 upon varying the WF from 4.6 to 4.0 eV, indicating that the WF has minimal effect on the current density of the HJSCs. According to the literature, the WF of ZnO-SnO_2 lies between 4.16 and 4.64 eV [14]. The effect of WF on the performance of the HJSCs was studied varying the WF from 4.6 to 4.0 eV and found to be significantly affecting the $\mathrm{V_{oc}}$ resulting in the increment in the magnitude from 0.0598 V at 4.6 eV to 0.658 V at 4.0 eV. If we could optimize the WF of ZnO-SnO_2 to 4.0 eV and the $\mathrm{N_A}$ to 10^{13} cm^{-3}, efficiency over 17% could be achieved. This knowledge is beneficial for the solar photovoltaic market in the development of the solar cell.

Figure 11.4 depicts the effect of the WF on the PCE of the junction solar cells. For semiconductor with high WF, N_A does not significantly affect PCE. Whereas for smaller WF, the effect of WF on the conversion efficiency is very significant.

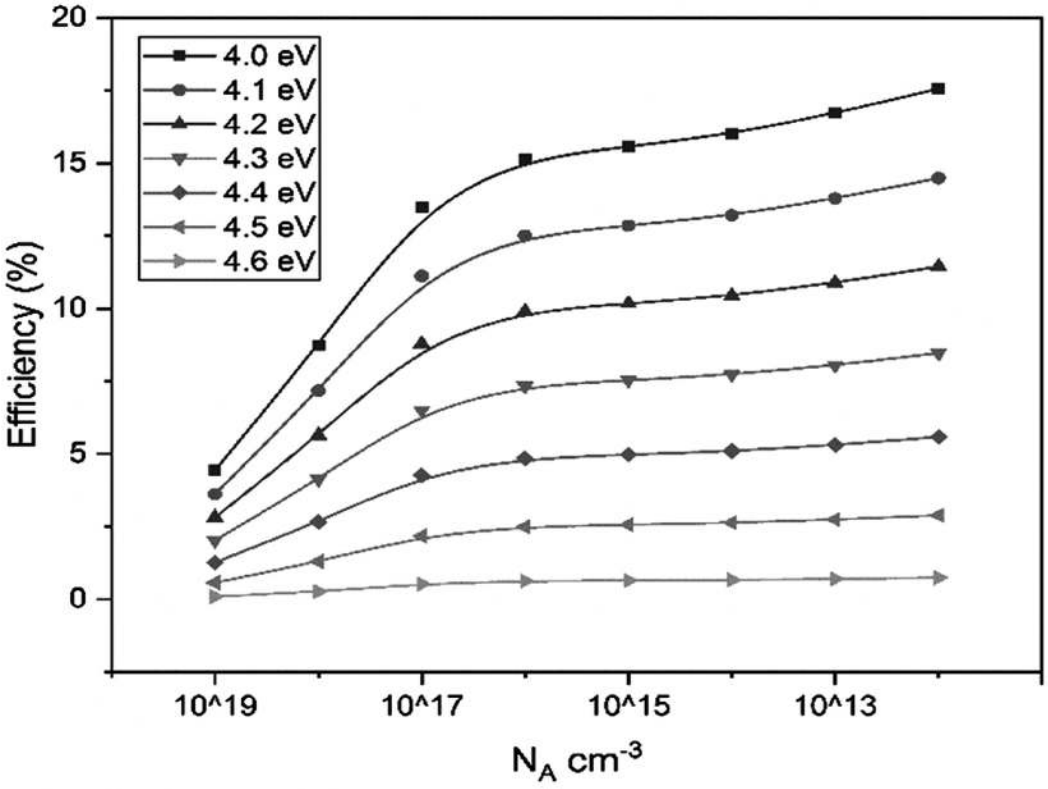

FIGURE 11.4 Power consumption efficiency vs N_A for different work function.

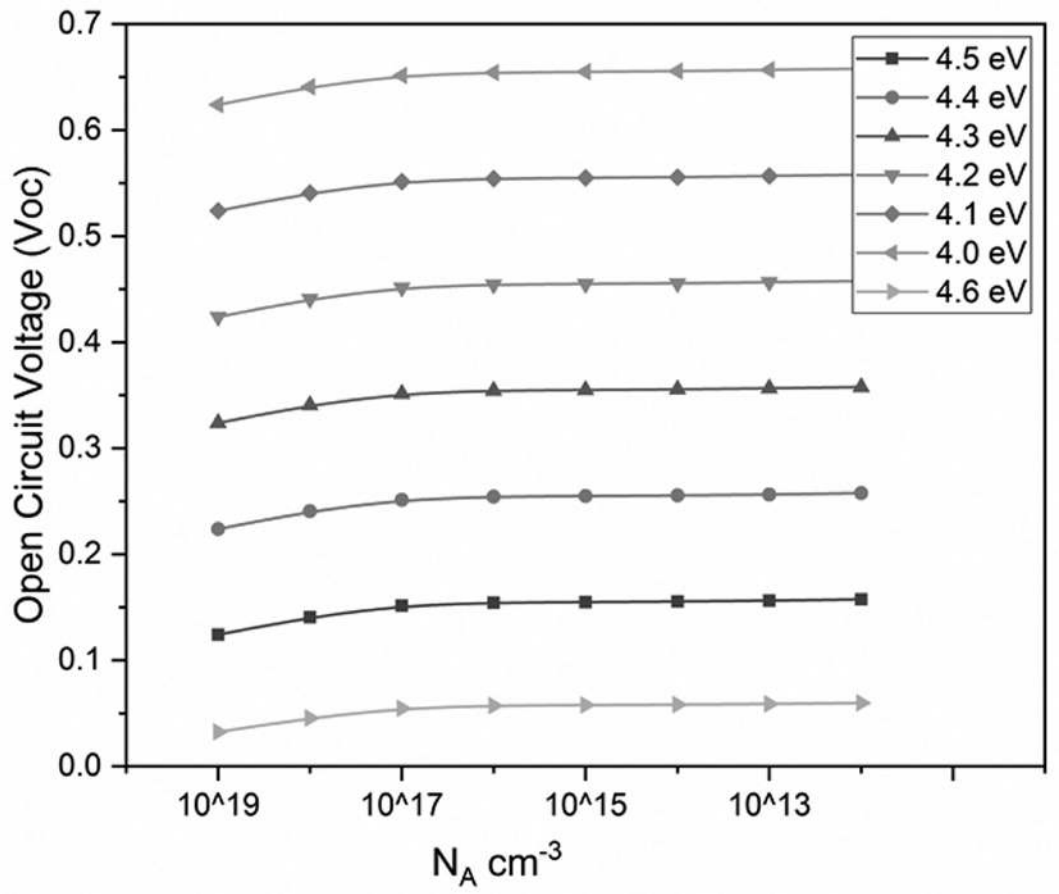

FIGURE 11.2 Open circuit voltage vs N_A for different work function.

It is to be noted that for the concentration greater than 10^{16} cm^{-3}, the conversion efficiency significantly reduced from 15.45 to 4.43%. This suggests that for the carrier concentration higher than 10^{18} cm^{-3}, as in our case confirmed from the hall measurement, the WF of the semiconductor can play a vital role in the performance of the devices. It is observed that the PCE reduces dramatically for lower values of WF.

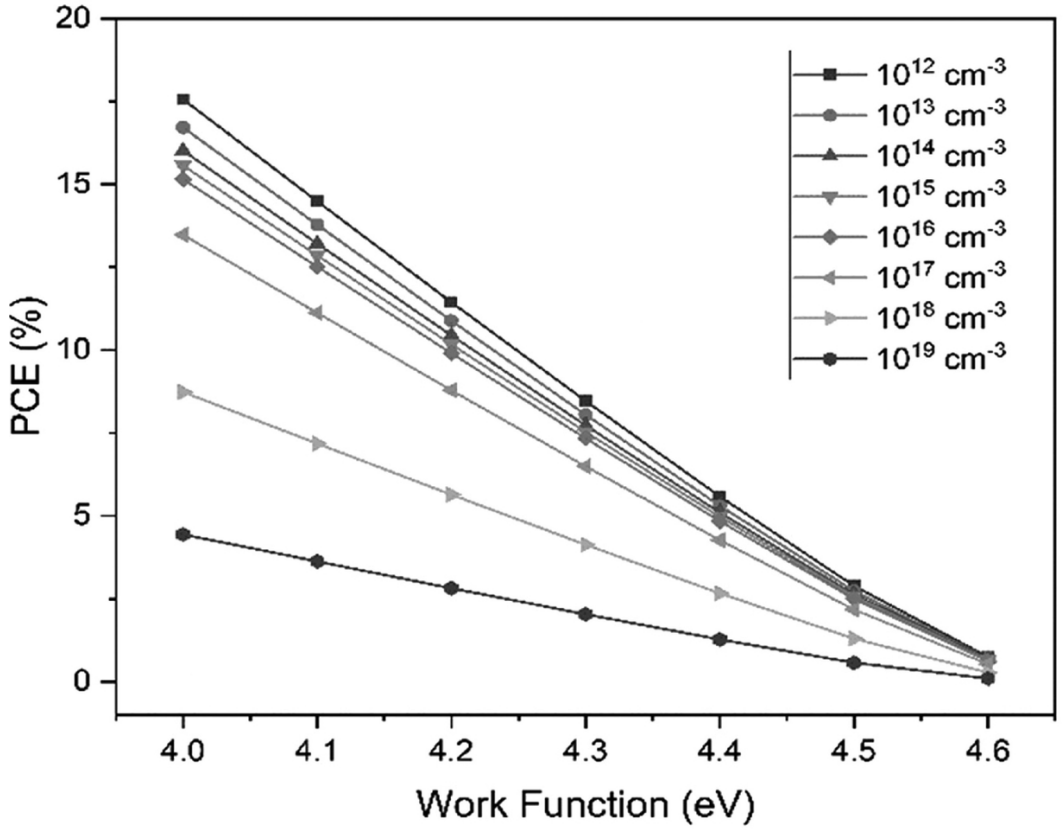

FIGURE 11.3 Power consumption efficiency vs work function.

It is to be noted that when there is increment in WF, the value of PCE is reduced. In addition the variation in the PCE for WF greater than 4.5 eV is insignificant. For the small WF, we can play with the conversion efficiency of the HJSCs by minimal variation in the WF significantly increasing the efficiency of the cell. It can be seen that the tuning of WF from 4.6 to 4.0 eV facilitated the increment in the V_{oc} from 0.0598 to 0.658 V, the major reason behind the enhanced efficiency resulting in the photo-conversion efficiency from 0.74 to 17.56%.

11.4 CONCLUSION

In this chapter, the effect of bulk semiconductor properties on the important cell parameters including short V_{oc}, J_{sc}, FF, and PCE has been investigated thoroughly. It is observed that the WF of the semiconductor has a

significant effect on V_{oc} resulting in the increment in the value of V_{oc} from 0.0598 to 0.658 V upon the variation of WF from 4.6 to 4.0 eV, resulting in the increment in the efficiency of the HJSCs from 0.738 to 17.56%. Whereas there is insignificant variation in the short circuit current upon variation of WF. The present study finds very important possibility in tuning the performance of the solar cell through materials bulk properties for enhanced efficiency for the future photovoltaic market.

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KEYWORDS

- **heterojunction**
- **optoelectronics**
- **power conversion efficiency**
- **work function**
- **ZnO-SnO_2**

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CHAPTER 12

Design and Comparative Analysis of Different Geometric Structures of Micro-Cantilever Diaphragm for Biosensor Application

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ABSTRACT

Researchers and scientific community have been motivated by current trends in the area of biosensing for development of cost effective bio analytical instruments that are label-free and miniaturization of the same. Biosensors are chemical sensing devices that quantify or detect biological molecule. In this chapter a comparison of two different structures of the micro-cantilever beams for the application in biosensing has been demonstrated. The proposed devices have been tested considering the HIV

molecules as the target analyte that works on the mechanism of the displacement due to adsorption and absorption between HIV molecule and the diaphragm. The proposed device was designed using COMSOL Multiphysics. The diameter of the circular diaphragm was considered to be 150 µm and the size of the square diaphragm was 84.64 μm^2. To investigate the effect of length and width of the cantilever on biosensing application, the length and width were varied from 200 to 400 µm and from 75 to 150 µm, respectively. The geometric dimensions with the best deflection that can be employed in micro-cantilever biosensor applications are circular diaphragm having length 400 µm and width 75µm showing a displacement of 12.95 µm.

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12.1 INTRODUCTION

Micro-cantilever sensors have gained the attention in recent years because of its demand as a platform for the development of a wide range in the field of physical, chemical, and biological sensing [1, 2]. In addition to that, micro-cantilevers are highly sensitive to specific bio/chemical target analytes, label-free platform for its realtime detection of analytes [3], and easy to fabricate anduse [4]. Furthermore, it also has potential to detect the target elements in hazardous places and harmful toxin substances [5].

Acquired immunodeficiency syndrome (AIDS) caused by human immunodeficiency virus (HIV) was first reported in US center for disease control in 1981 [6], and it transmitted through unsafe sex, use of non-sterile syringes and tools, blood transfusion, and so forth [7]. Till date the world has been suffering from deadly AIDS with more than 85.6 million infected

[8]. There exist several testing and diagnosis methods for HIV infection, such as nucleic act test (NAT) [9] and enzyme linked through immunosorbent assay (ELISA) [10], and so forth. However, these methods come up to be very expensive and complex [11, 12], motivating the researchers and scientific community in finding simpler and cost effective techniques. In this direction, we simulated a micro cantilever-based biosensor for HIV detection.

A cantilever is a typical mechanical structure that has one end constrained and the other end free that operates under static mode sensing and dynamic or vibration mode sensing principles. In static mode, basically, there is a coated sensing layer that is specific to binding the target analyte [12]. In the present work, the diaphragm is employed as the sensing absorption of the target layer depicted in Figure 12.1. Due to the absorption of the target analyte in the scanning region, a new molecular layer is formed, and due to this, a stress is produced on the micro-cantilever beam, causing the beam to deform [13].

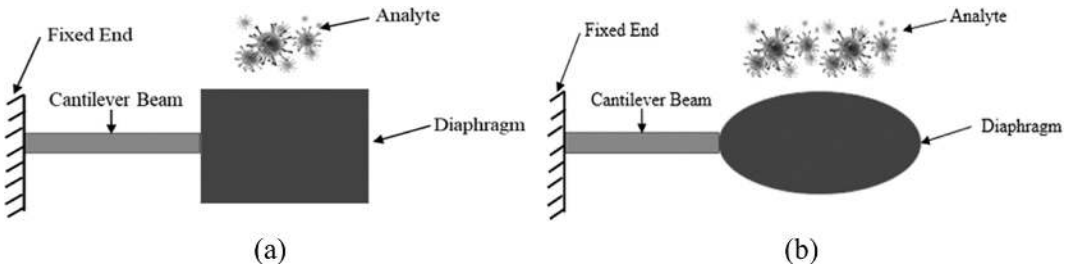

FIGURE 12.1 Micro cantilever-based biosensor with, (a) square diaphragm and (b) circular diaphragm.

The structure of HIV differs from that of other retroviruses [14], whose shape is spherical with a diameter of 126 nm, and one HIV molecule produces a total force of 9.8×10^{-18} N on the surface [14].

12.2 DESIGN AND METHOD

The mechanism of biosensing application using micro-cantilever is based on the principle of converting bio recognition into nano mechanical motion upon the exposure of targeted specimen or the analytes attributed to the change in free energy on the surface of the cantilever generated by the reaction of the target analyte with the probe coating molecules. The probe coating is a chemically sensitive layer that enables analyte specificity [15]. For the detection of a specific analyte, the micro-cantilever transducer is designed with probe coating on the surface based on analyte's nature. In the present work, two distinct diaphragm structures, namely the circular and square have been considered for the application in biosensing with the target sample to be considered as HIV molecules [16, 17]. In both the structures under consideration, one end is fixed while the other end is the square and the circular diaphragm as depicted in Figure 12.2(a) and (b), respectively. To design the 3D model of the structure, the model wizard as spatial dimension has been chosen. It was then followed by the selection of solid mechanics as the study parameters for the deflection analysis. The material properties of the sensor under consideration for the simulation are summarized in Table 12.1.

TABLE 12.1 Material Properties of Silicon. ⏎

Properties	**Value**
Young's modulus	140 (Gpa)
Poisson's ratio	0.265
Density	2.38×10^{-6} kg/m^3

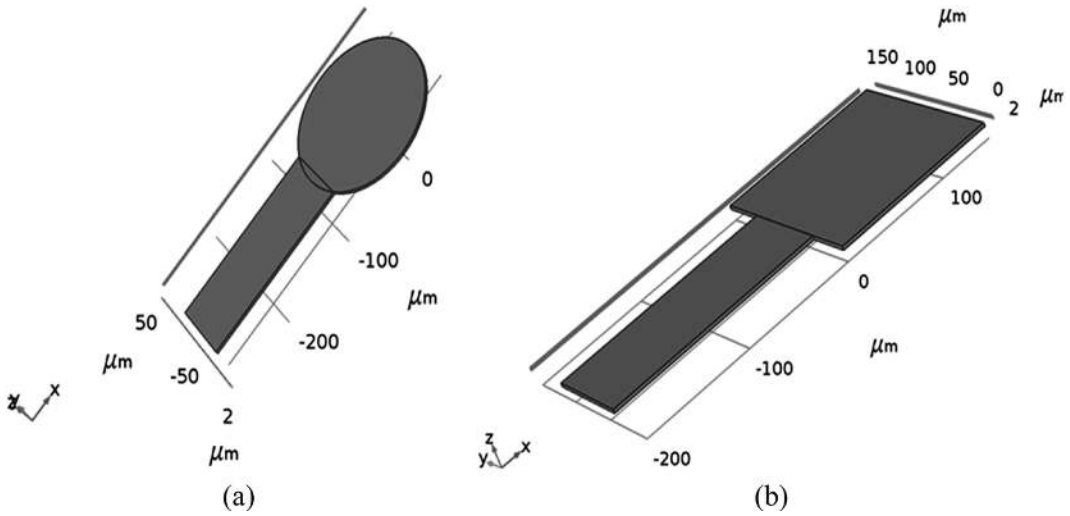

FIGURE 12.2 Design of rectangular shape micro-cantilever beam, (a) circular and (b) square diaphragm.

Further, the surfaces of both diaphragms are assumed to be coated with HIV antibodies. According to Gopinath et al. [14], equivalent force produced by one molecule of HIV is 9.8×10^{-18} N. When a clinical sample with HIV positive is exposed to the surface of the diaphragm, antigenantibody interaction happens resulting to surface tension disturbance and causing nano mechanical motion in terms of micro-cantilever beam displacement.

12.3 RESULT AND DISCUSSION

In this work, we assume that one HIV molecule is completely absorbed in the surface of diaphragm producing 9.8×10^{-18} N downward force on the diaphragm surface. In considering the circular diaphragm to investigate the effect of the length of cantilever in biosensing application, the length was varied from 200 to 400 μm. The result (Figure 12.3) revealed that the displacement or dispersion increases monotonically with the length of the cantilever, suggesting the choice of the longer cantilever for better biosensing application.

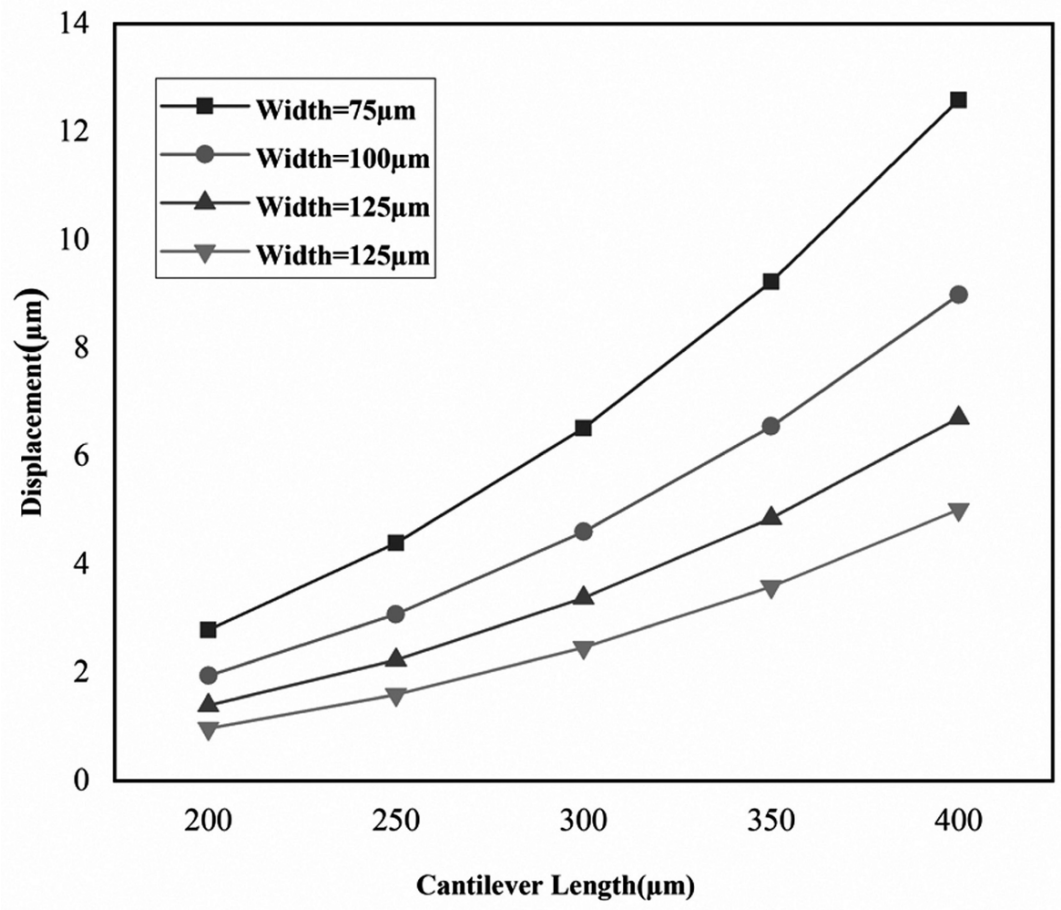

FIGURE 12.3 Displacement of micro-cantilever width variation from 75 to 150 µm.

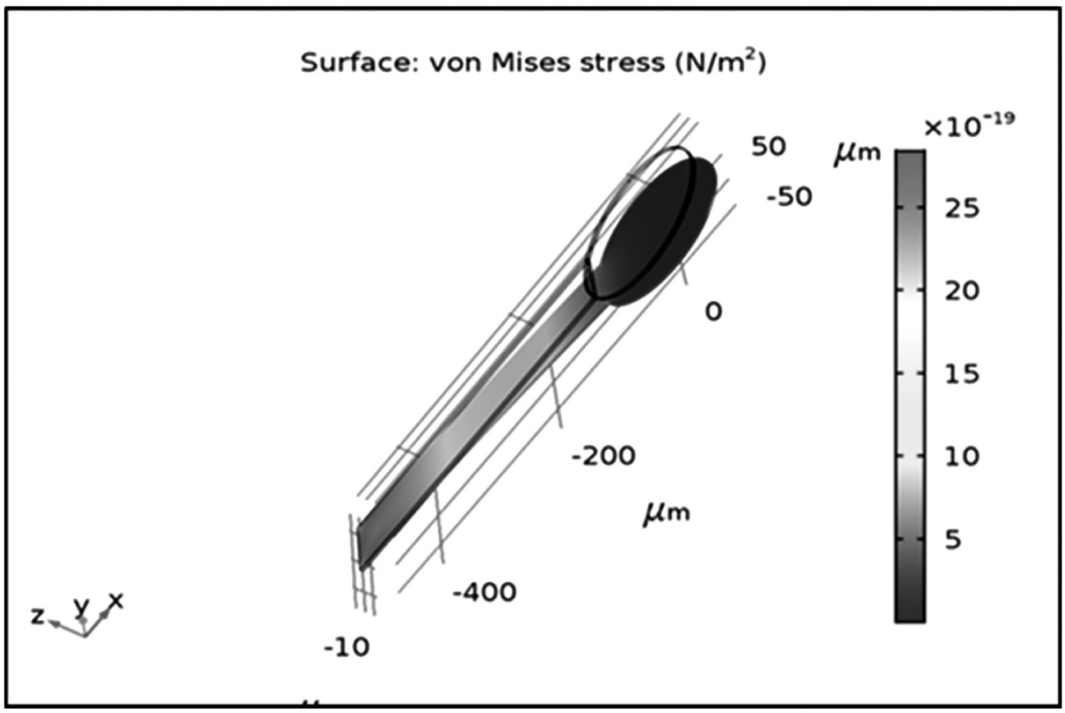

FIGURE 12.4 12.59 μm deflection of micro-cantilever after exposing the HIV molecule on surface of circular diaphragm for micro-cantilever having length 400 and width 75 μm.

Similarly, for the square diaphragm the length of the cantilever was varied from 200 to 400 μm in steps of 50 μm. Figure 12.5 depicts the result of the displacement of the micro-cantilever upon exposure of the HIV molecule. The result varies in the micro-cantilever upon exposure of the HIV molecule. The results vary in the fashion, that is, displacement increases monotonically with the length of diaphragm.

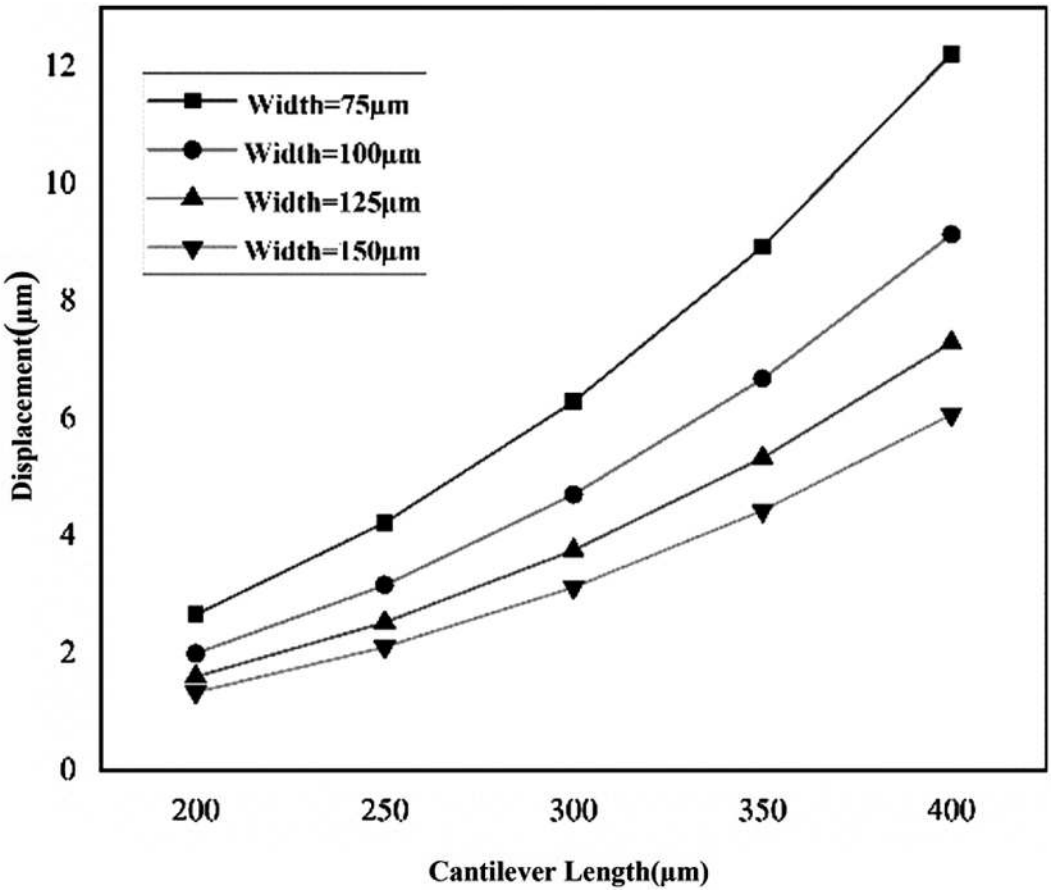

FIGURE 12.5 Displacement of micro-cantilever with square diaphragm width variation from 75 to 150 µm.

12.4 CONCLUSION

This chapter presents the design of micro-cantilever sensor for comparative analysis of various geometric structures for biosensor application. It is to be noted, for a sensor with a width of 75 µm and a length of 400 µm, the circular diaphragm-based sensor proved to be more effective, showing a displacement of 12.59 µm as compared to the square diaphragm's 12.21 µm. The result suggests that this sensor can detect a tiny force of 9.8×10^{-18} N, corresponding to the weight of an HIV molecule.

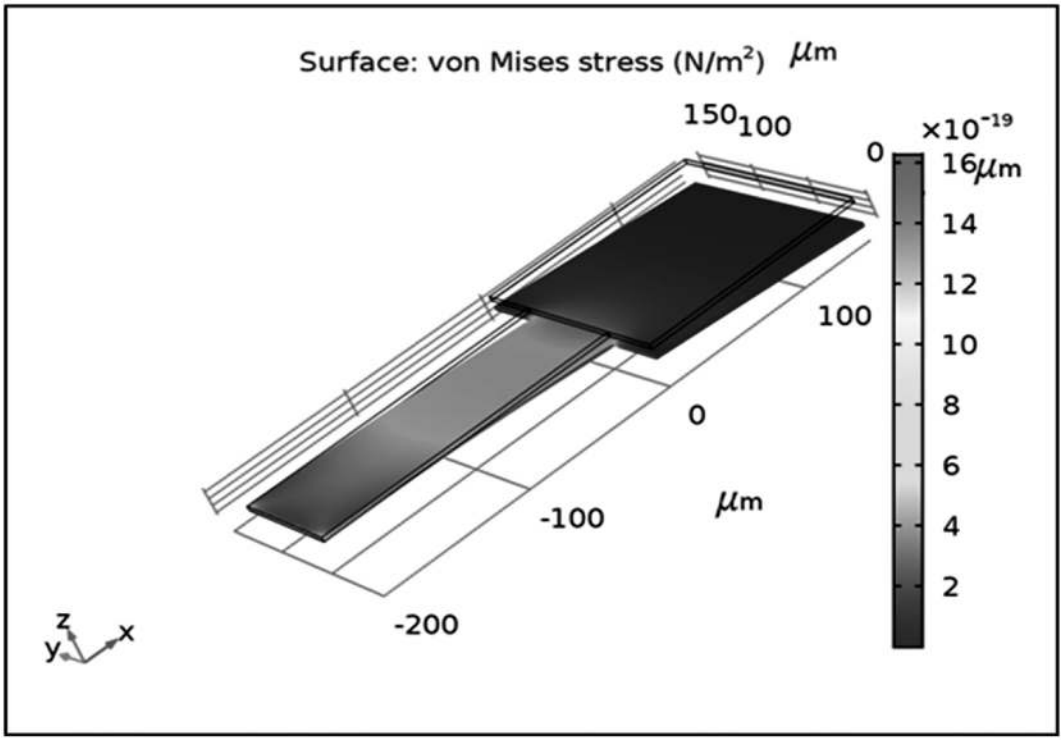

FIGURE 12.6 12.21 μm Deflection of micro-cantilever after exposing the HIV molecule on surface of square diaphragm for micro-cantilever having length 400 and 75 μm width.

The research makes a significant contribution to developing costeffective, label-free, and small bioanalytical tools for detecting HIV. It highlights the potential of micro-cantilever sensors in various biosensing roles, detecting changes in cantilever bending for physical, chemical, or biological sensing. The study also emphasizes the need to improve the design of micro-cantilever sensors to make them work better for biosensing.

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KEYWORDS

- **analyte**
- **biosensor**
- **diaphragm**
- **micro-cantilever**
- **nano mechanical motion**
- **static mode sensing**
- **vibration mode sensing**

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CHAPTER 13

Design of a Sensitivity Improved Surface Plasmon Resonance (SPR) Sensor with Barium Titanate ($BaTiO_3$) and Blue Phosphorus-Tungsten Disulphide (BlueP-WS_2)/Black Phosphorous (BlackP) Hybrid Structure

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ABSTRACT

This chapter is aimed at enhancing the sensitivity of a conventional surface plasmon resonance (SPR) sensor based on BK7 prism and gold (Au) using a combination of different novel materials. Various designs of SPR sensors are presented utilizing novel materials, such as $BaTiO_3$, BlueP-WS_2 heterostructure, and BlackP, showcasing improved sensitivities than the conventional SPR sensor. The multi-layer structure of the SPR sensors is developed using the transfer matrix method (TMM). The sensor performances are examined with respect to three key factors: full width at half maximum (FWHM), sensitivity, and quality factor (QF). The thickness of Au, $BaTiO_3$ and layers of BlueP-WS_2 heterostructure, and BlackP is

optimized to yield maximum sensitivities at a working wavelength of 633 nm in the refractive index range (1.33–1.335 RIU) of the sensing layer. Design IV (proposed sensor) produces the maximum sensitivity of 280°/ RIU with 56 nm Au, 1.6 nm $BaTiO_3$, trilayer of BlueP-WS_2 (2.25 nm), and seven layers of BlackP (3.71 nm) along with QF and FWHM of 45.54 RIU^{-1} and 6.14812°, respectively.

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13.1 INTRODUCTION

Surface plasmon resonance (SPR) is used as an important label-free and sensitive optical detection tool to measure refractive index (RI) changes of the sensing layer. It finds diversified applications across fields, such as drug detection, medical diagnostics, to food safety, and so forth. [1, 2 and 3]. Different configurations of instrumentation ranging from prism-coupled to fiber-optic have been utilized over the years for SPR-based sensing applications. Optical fibers have certain limitations, such as they are prone to breakage and also have the problems of coating multiple layers over it for sensitivity improvement [4, 5]. The prism-based SPR sensors in comparison show enhanced sensitivity and stability. Therefore, the Kretschmann angular interrogation mode of scheme is the most preferred scheme compared to all other modes of SPR sensing [6]. It uses a prism coated with a suitable thickness of metal to let light from a p-polarized light source pass through which creates an evanescent wave that permeates the surrounding medium. A state of resonance, which is the reduction in the intensity of the light reflected, occurs when the surface plasmon (SP) wave interacts with the evanescent wave at a certain incident angle termed as the resonance angle. The resonance condition is influenced by the wavelength of the incident light, angle of incidence, RI, and thicknesses of the dielectric and metal layer.

Considerable effort is focused toward the use of novel materials for further enhancement of SPR sensitivity based on silver (Ag) and gold (Au) [7, 8]. 2D nanomaterials, namely black phosphorus, transition metal dichalcogenides

(TMDCs), heterostructures, and so forth owing to their superior properties, such as charge transfer, work function, high energy bandgap, large surface area to volume ratio, optical absorption capacity, and so forth have attracted significant attention for enhancement of SPR sensitivity [9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24 and 25]. Table 13.1 enlists the RI (at 633 nm) and monolayer thickness of heterostructures of 2D nanomaterials reported in SPR sensing [26, 27]. Metal oxides with high values of RI, namely barium titanate ($BaTiO_3$), titanium dioxide (TiO_2), and so forth have garnered attention for improving performance of SPR sensors in addition to heterostructures of 2D nanomaterials. Metal oxides with high values of RI in combination with plasmonic metals support the strong excitation of SPs for enhancing SPR sensitivity [28, 29, 30, 31, 32, 33 and 34]. Table 13.2 enlists the RI (at 633 nm) of different metal oxides reported in SPR sensors over the years [35, 36]. Besides, the RI of the glass prism significantly impacts SPR performance. The use of prisms with lower RI results in SPR sensors with higher sensitivity compared to higher RI prisms at a relevant visible wavelength. However, in comparison to higher RI prisms, prisms having low RI narrow the dynamic range of detection and in addition also hamper the measurement precision in sensing due to widening of the FWHM. Table 13.3 enlists the RI (at 633 nm) of different glass prisms used in SPR based sensing over the years [37].

TABLE 13.1 RI and Single Layer Thickness of Heterostructures of 2D Nanomaterials and Their Use in SPR Sensing.

2D Nanomaterials and Their Heterostructures	Thickness of Single Layer (nm)	RI
MoS_2	0.65	5.0805+1.1724i
$MoSe_2$	0.70	4.6226+1.0062i
WS_2	0.80	4.8937+0.3123i
WSe_2	0.70	4.5501+0.4332i
Graphene	0.34	3.0+1.1487i

2D Nanomaterials and Their Heterostructures	Thickness of Single Layer (nm)	RI
MXene	0.993	2.38+1.33i
BlueP-$MoSe_2$	0.78	2.770+0.350i
BlueP-MoS_2	0.75	2.810+0.320i
BlueP-WSe_2	0.78	2.680+0.220i
BlueP-WS_2	0.75	2.480+0.170i

TABLE 13.2 RI of Different Metal Oxides Used in SPR Sensing.

Glass Prism	RI
ZnO	1.952+0.02i
TiO_2	2.5836
$BaTiO_3$	2.4042

TABLE 13.3 RI of Different Glass Prisms Used in SPR Sensing.

Glass Prism	RI
CaF_2	1.4329
FK51A	1.4853
BK7	1.5150
SF10	1.72312
SF11	RI 1.77858

This chapter proposes the design of a Kretschmann angular configured SPR sensor with improved sensitivity based on six layer arrangements consisting of a mixture of 2D nanomaterials, heterostructures of different 2D nanomaterials, oxides, and Au as the plasmonic metal. The working of the sensor is governed at a working wavelength of 633 nm for 1.33–1.335 RIU. Section 13.2 presents the theory of SPR sensing, arrangement of different layers and the design consideration of the sensor proposed in this chapter, and the performance evaluating parameters. Section 13.3 discusses the results elaborately. The conclusion is provided in Section 13.4.

13.2 METHODOLOGY

13.2.1 SENSOR THEORY AND MATHEMATICAL MODELING

The combined oscillation of a metal's free electrons with regard to stationary positive ions is known as a plasmon. The combined oscillations of the conduction electrons throughout the interface of metal-dielectric are known as SPs. The collective electron density wave traveling throughout the interface of metal-dielectric is referred to as the surface plasmon wave (SPW). The schematic illustration of the SPs traveling along the metaldielectric interface is represented in Figure 13.1.

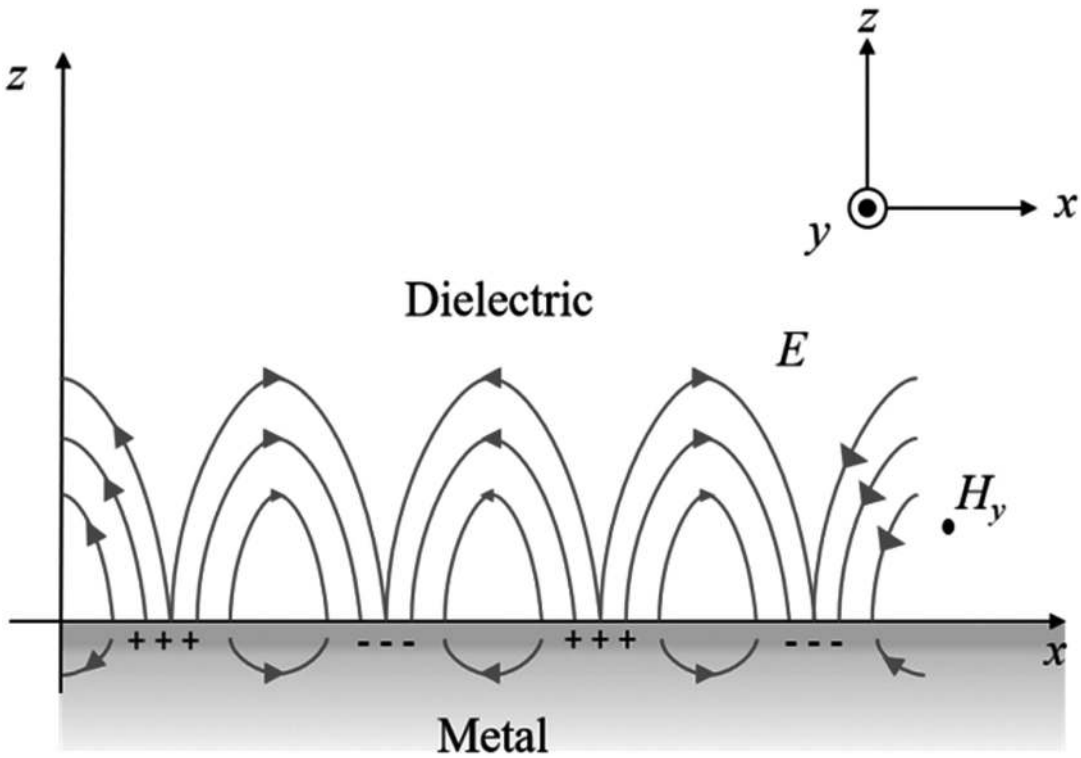

FIGURE 13.1 Schematic representation of SPs electromagnetic field traveling throughout the interface of metal-dielectric.

The SPW propagation constant (K_{SP}) is represented as described in Ref [38]:

$$K_{SP} = \frac{\omega}{c}\left[\sqrt{\frac{\epsilon_M \epsilon_s}{\epsilon_M + \epsilon_s}}\right] \tag{13.1}$$

where c is the light's velocity, ω is its incidence frequency, and ϵ_M, ϵ_S stand for the metal layer's and the dielectric medium's respective dielectric constants. There

is a momentum mismatch between the propagation constant of SPW and the light wave with p-polarization in a dielectric medium. Hence, SPs at a metal-dielectric interface cannot be excited using direct light. Therefore, to match the evanescent wave to the SPs, a prism is used to enhance the light wave vector and momentum. This is accomplished using the Kretschmann configuration by making a light source with p-polarization hitting the sensor traveling through a prism. A detector is then used to gather the entire amount of internally reflected light. An evanescent wave is generated at this point whose propagation constant (K_{ev}) is given by [38]:

$$K_{ev} = \frac{\omega}{c} n_p \sin\theta \tag{13.2}$$

where ω, θ, n_p, and c stand for light's frequency, incident angle, the glass prism's RI, and light's speed, respectively.

SPs excitation is achieved when wave vector of the evanescent wave's propagation constant coincides with the wave vector of the SPW with a comparable polarization state and frequency. This happens at a particular incidence angle, Θ_{SPR}. The equation below provides the associated resonance condition [38]:

$$\frac{\omega}{c} n_p \sin\theta_{SPR} = \frac{\omega}{c}\left[\sqrt{\frac{\epsilon_M \epsilon_s}{\epsilon_M + \epsilon_s}}\right] \tag{13.3}$$

The Drude-Lorentz model is applied to determine the metal's (Au) dielectric constant; providing the relationship between the wavelength and the metal's dielectric constant (ϵ_M), as shown below [39]:

$$\epsilon_m(\lambda) = 1 - \left[\frac{\lambda^2 \lambda_C}{(\lambda_C + i\lambda)\lambda_p^2}\right] \tag{13.4}$$

where the Au collision wavelength (λc) is 8.93×10^{-6} m and the plasma wavelength (λp) is 1.68×10^{-7} m.

The current study evaluates the SPR sensor's reflectance curve based on the transfer matrix method (TMM) and Fresnel multilayer reflection theory.

The electromagnetic field boundary's tangential components are listed as described in Ref [40]:

$$\begin{pmatrix} P_1 \\ Q_1 \end{pmatrix} = X_1 X_2 X_3 X_4 X_5 \ldots\ldots\ldots\ldots\ldots\ldots X_{N-1} \begin{pmatrix} P_{N-1} \\ Q_{N-1} \end{pmatrix} = X \begin{pmatrix} P_{N-1} \\ Q_{N-1} \end{pmatrix} \tag{13.5}$$

At the first and final layer interfaces, the electric and magnetic fields tangential components are P_1, Q_1, and P_{N-1}, Q_{N-1}, respectively. The characteristic matrix X, having elements Xij, is described in Ref [40]:

$$X = \begin{bmatrix} x_{11} & x_{12} \\ x_{21} & x_{22} \end{bmatrix} = \prod_{k=2}^{N-1} X_k \tag{13.6}$$

$$\text{with } X_k = \begin{bmatrix} \cos\beta_k & -i\sin\beta_k/q_k \\ -iq_k\sin\beta_k & \cos\beta_k \end{bmatrix} \tag{13.7}$$

where k is an arbitrary number, and the associated layers' phase thickness and RI are represented by βk and qk, respectively. The transfer matrix elements are denoted by x_{11}, x_{12}, x_{21}, and x_{22}. q_k and β_k are listed as follows [40]:

$$q_k = \left[\frac{\left(\epsilon_k - n_p^2 \sin^2\theta\right)^{\frac{1}{2}}}{\epsilon_k} \right], \beta_k = \frac{2\pi d_k}{\lambda} \left[\left(\epsilon_k - n_p^2 \sin^2\theta\right)^{\frac{1}{2}} \right] \tag{13.8}$$

where the permittivity and thickness of the kth layer are indicated by ϵ_k and d_k, respectively.

The amplitude of the reflectivity (R_P) and reflection coefficient (r) for the light source which is incident in p-polarization are computed as described in Ref [40]:

$$R_p = \left| r \right|^2 = \left[\frac{(x_{11} + x_{12}q_N)q_1 - (x_{21} + x_{22}q_N)}{(x_{11} + x_{12}q_N)q_1 + (x_{21} + x_{22}q_N)} \right] \tag{13.9}$$

13.2.2 LAYER ARRANGEMENT

The proposed Kretschmann angular configured SPR sensor consists of six different layers arranged in the order, namely BK7 prism, Au, $BaTiO_3$, BlueP-WS_2, BlackP, and sensing medium whose schematic representation is shown in Figure 13.2. Table

13.4 enlists the arrangement of the layers along with their optimum thicknesses and RI implemented in the sensor proposed in this chapter.

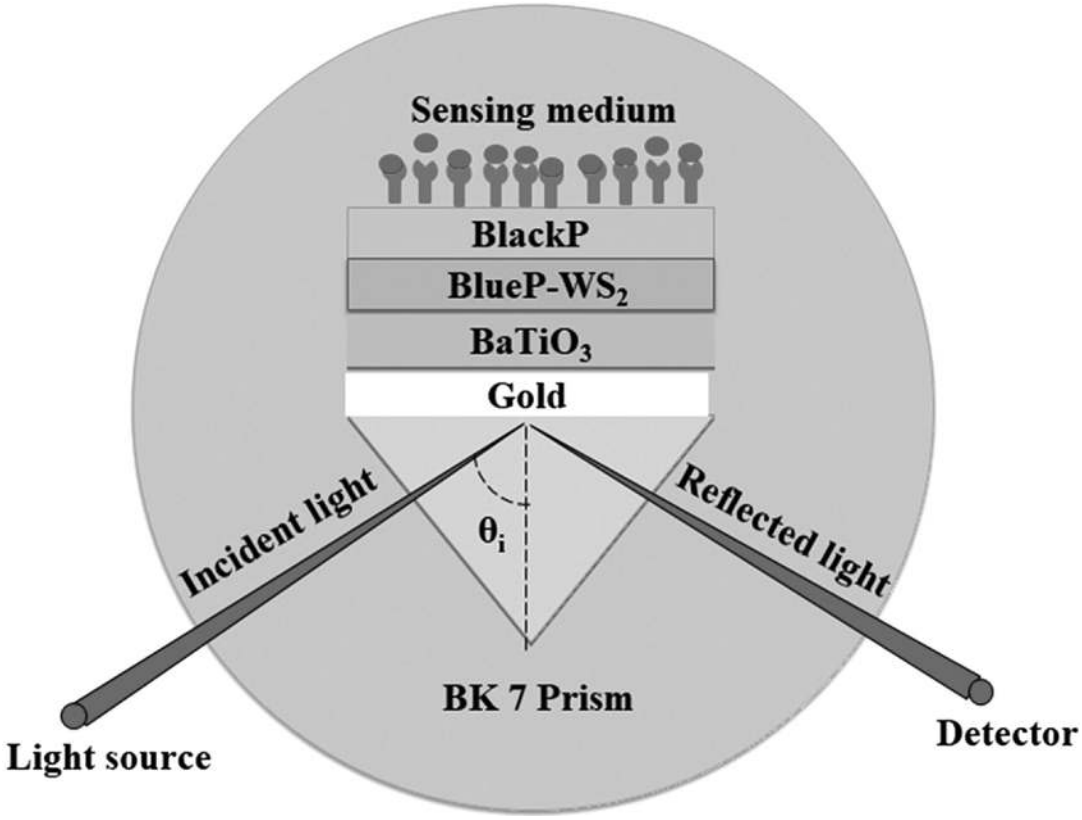

FIGURE 13.2 Schematic illustration of the sensor proposed in this chapter.

TABLE 13.4 Optimized Thickness and RI of Different Layers in the Sensor Proposed in This Chapter.

Layer	Materials	Optimized Thickness (nm)	RI (633 nm)
Layer No.1	BK7 Prism	–	1.5150 [37]
Layer No.2	Au	56	0.16172+3.21182i [37]
Layer No.3	$BaTiO_3$	1.6	2.4042 [41]
Layer No.4	BlueP-WS_2	2.25	2.480+0.170i [42]
Layer No.5	BlackP	3.71	3.5 [43]

Layer	Materials	Optimized Thickness (nm)	RI (633 nm)
Layer No.6	Sensing medium	–	1.330–1.335 [43]

13.2.3 CHOICE OF MATERIALS

The materials selected for the proposed sensor are listed as:

Glass prism

BK7 prism (RI of 1.515) is implemented as the first layer of the sensor, preferred because of its lower RI than prisms like SF10, SF11, and so forth, developing enhancement in SPR sensitivity. Besides, BK7 prism with a higher RI than prisms like CaF_2, FK51A, and so forth, also provides better detection accuracy for SPR measurement [37].

Metal layer

Au is utilized as the second layer as it exhibits higher resonance shifts with changes in RI of the sensing medium compared to Ag as well as due to its inertness [44, 45].

Oxide layer

$BaTiO_3$ is implemented as the third layer. It is a dielectric material which is preferred due to its low dielectric losses, high dielectric constant, and high RI favoring enhanced sensitivity of SPR sensor [41].

Heterostructure layer

BlueP-WS_2 heterostructure is the fourth layer. Both BlueP and WS_2 have hexagonal lattice structures with lattice constants of 3.268 and 3.295 Å, respectively, having a small interlayer mismatch of 3.15% which is in an acceptable range for the experimental synthesis of the heterostructures [46].

2D nanomaterial layer

BlackP is used as the fifth layer due to its high RI favoring the increased sensitivity of SPR sensor [43].

Sensing layer

With a RI of 1.330–1.335, the sensing medium serves as the sixth layer [43].

Light source

Monochromatic source of light with wavelength 633 nm is preferred due to increment of optical nonlinearity at high frequencies and enhanced SPR sensitivity with reduced Kerr effect [39].

Table 13.5 enlists the structure of different SPR sensor designs considered in this chapter. The TMM and Fresnel multilayer reflection theory was implemented to plot the SPR reflectance curves. The investigation of the performance characteristics of the sensors was done using a MATLAB simulation program using a graphical analysis approach [40].

TABLE 13.5 Structure of Different SPR Sensor Designs.

Design	Orientation of the Layers
Design I	Layer 1:BK7prism, Layer 2:Au, Layer 3:Sensing layer
Design II	Layer 1:BK7prism, Layer 2:Au, Layer 3:BlueP-WS_2, Layer 4:Sensing medium
Design III	Layer 1:BK7prism, Layer 2:Au, Layer 3:$BaTiO_3$, Layer 4:BlueP-WS_2, Layer 5:Sensing layer
Design IV (proposed)	Layer 1:BK7 prism, Layer 2:Au, Layer 3:$BaTiO_3$, Layer 4:BlueP-WS_2, Layer 5: BlackP, Layer 6:Sensing layer

13.2.4 PERFORMANCE EVALUATING PARAMETERS

The proficiency of SPR performance is evaluated using sensitivity (S), FWHM, and quality factor (QF).

Sensitivity (S), expressed in °/RIU, is described as the ratio of the shift of SPR angle ($\Delta\Theta$) to the variation in sensing medium RI (Δn) [47].

$$\mathrm{S} = \frac{\Delta\Theta}{\Delta n} \tag{13.10}$$

FWHM of an SPR sensor, represented in degrees (°) represents the line width of the SPR reflectance curve [48]. A narrow FWHM indicates a SPR sensor having a high accuracy in detection of resonance angle.

QF of an SPR sensor, represented in RIU^{-1} is expressed as the ratio of the sensitivity and FWHM [49].

$$\mathrm{QF} = \frac{\mathrm{S}}{\mathrm{FWHM}} \tag{13.11}$$

A good SPR sensor is indicated by a high QF value.

13.3 RESULTS AND DISCUSSION

There are three distinct subsections within this section. The optimal thicknesses of various materials for improved performance of different SPR sensor designs are presented in Section 13.3.1. Section 13.3.2 presents a comparative study of the different designs. Section 13.3.3 provides a comparative performance analysis of the sensor proposed in this chapter with respect to some of the reported SPR sensors.

13.3.1 OPTIMIZATION OF THICKNESS

Design I

Design I consists of BK7 prism, Au, and sensing layer. The schematic representation of Design I is represented in Figure 13.3. The changes in performance measuring parameters with variation in Au thickness for Design I are represented in Table 13.6 and Figure 13.4. It is observed from the figure that the maximum sensitivity of 172°/RIU with QF of 40.35 RIU^{-1} and a low FWHM of 4.26311° is produced at 55 nm Au.

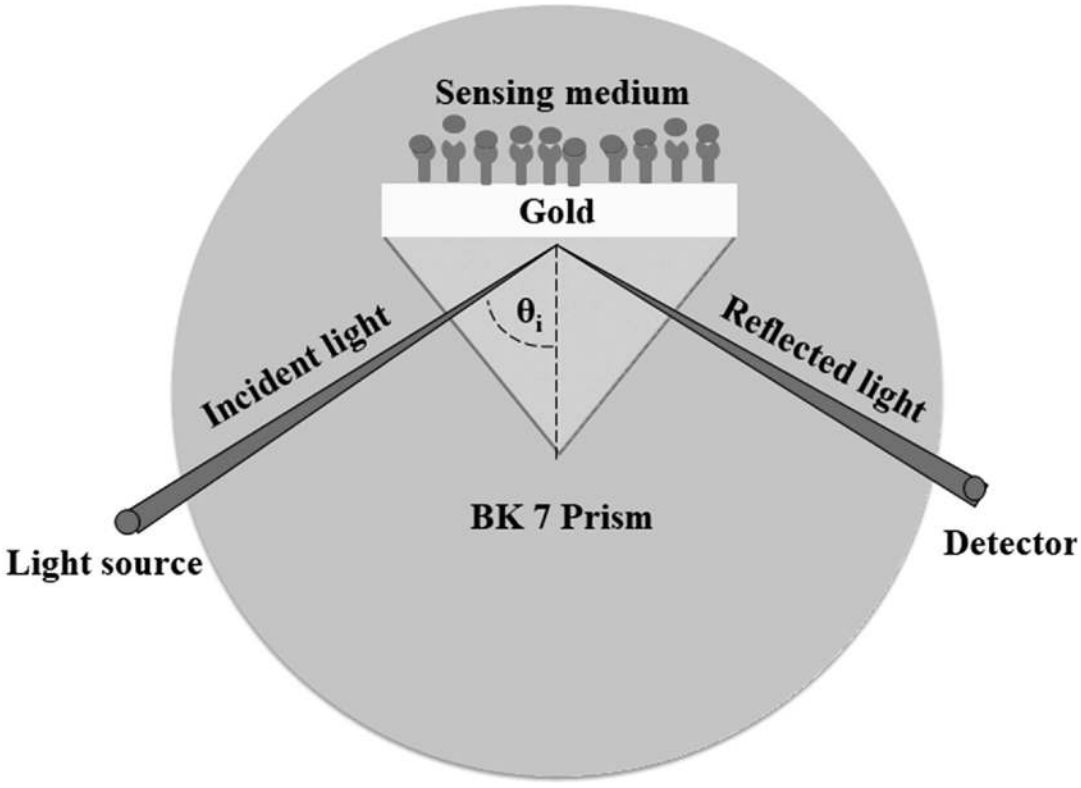

FIGURE 13.3 Schematic representation of Design I.

TABLE 13.6 Performance Measuring Parameters with Variation in Gold Thickness for Design I.

Thickness (nm)	Sensitivity (°/RIU)	FWHM(°)	QF (RIU^{-1})
35	136	7.676555	17.72
40	146	5.776575	25.27
45	156	5.118485	30.48
50	164	4.584995	35.77
55	172	4.26311	40.35

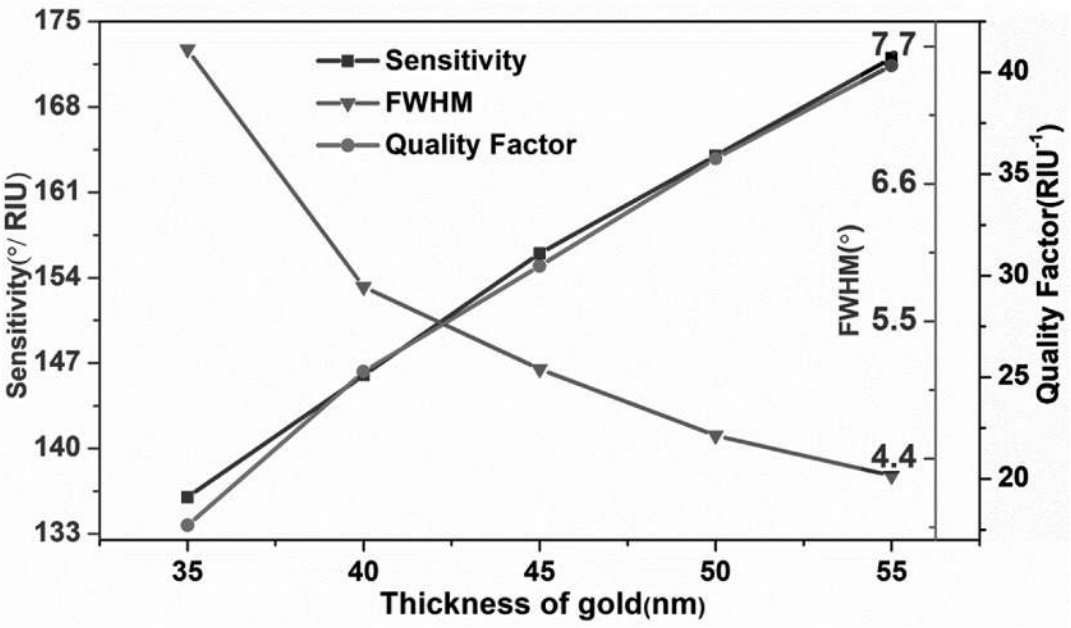

FIGURE 13.4 Change in the performance measuring parameters with increase in thickness of gold for Design I.

Design II

In Design II, a heterostructure of BlueP-WS_2 is placed over Au. The schematic representation of Design II is represented in Figure 13.5. The changes in performance measuring parameters with increment in BluePWS_2 layers for Design II are represented in Table 13.7 and Figure 13.6. The figure illustrates that the maximum sensitivity of 230°/RIU with FWHM of 4.86336° and QF of 47.29 RIU^{-1} is produced at trilayer thickness of BlueP-WS_2 (2.25 nm) for Design II.

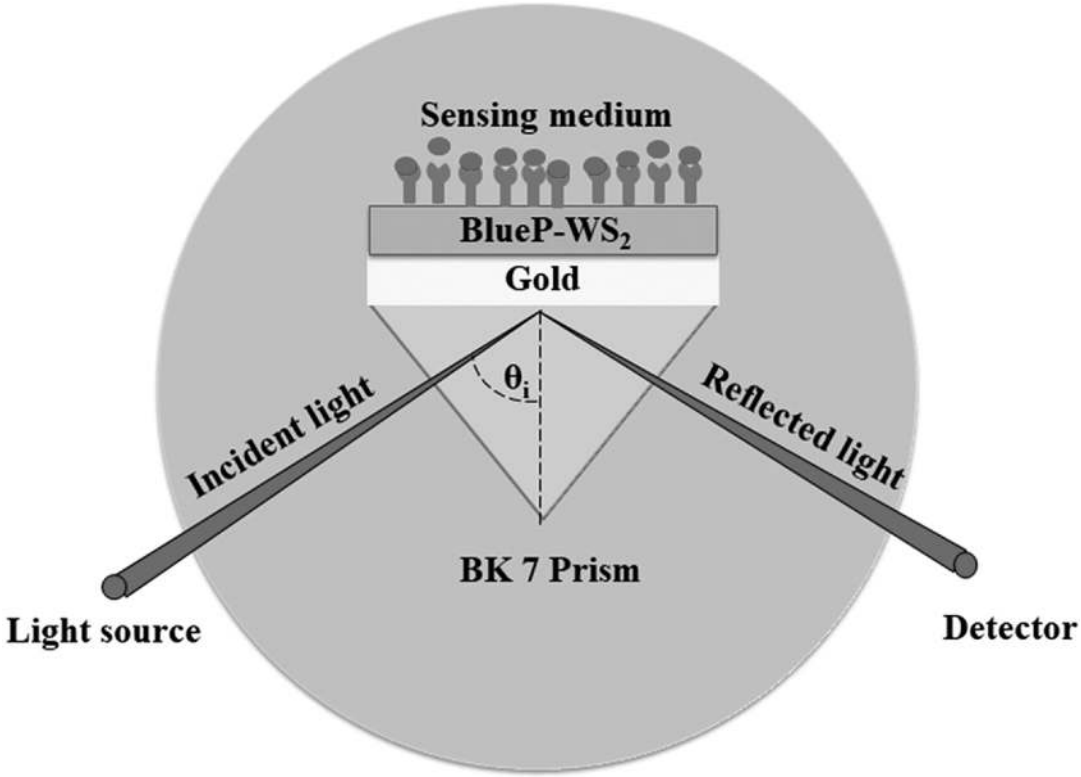

FIGURE 13.5 Schematic representation of Design II.

TABLE 13.7 Performance Measuring Parameters with Increment in BlueP-WS_2 Layers for Design II.

BlueP-WS2 Layers	Sensitivity (°/RIU)	FWHM(°)	QF (RIU^{-1})
1	188	3.85923	48.71
2	206	4.34431	47.41
3	230	4.86336	47.29
4	212	4.89213	43.33

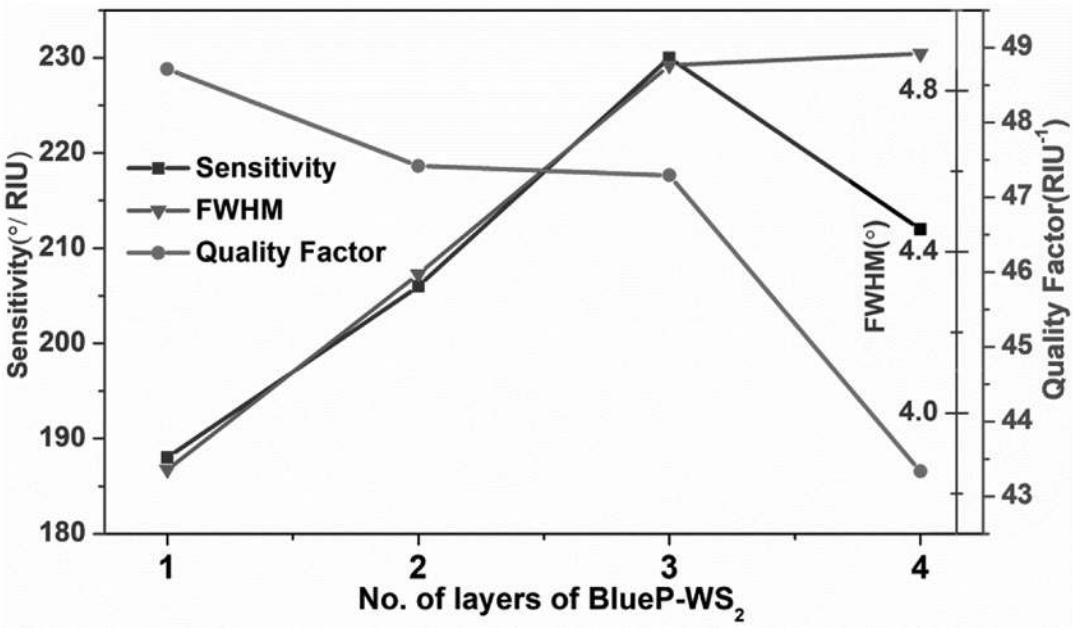

FIGURE 13.6 Change in the performance measuring parameters with increment in BlueP-WS_2 layers for Design II.

Design III

For modeling Design III, $BaTiO_3$ oxide is introduced between Au and BlueP-WS_2 heterostructure. The schematic representation of Design III is represented in Figure 13.7. The changes in performance measuring parameters with increment in BlueP-WS_2 layers for Design III are represented in Table 13.8 and Figure 13.8. The optimized thicknesses of Au and $BaTiO_3$ for Design III are determined to be 56 and 1.6 nm, respectively. Figure 13.8 indicates that the maximum sensitivity of 260°/RIU with FWHM and QF of 5.89366° and 44.1 RIU^{-1}, respectively is produced at trilayer thickness of BlueP-MoS_2 (2.25 nm) for Design III.

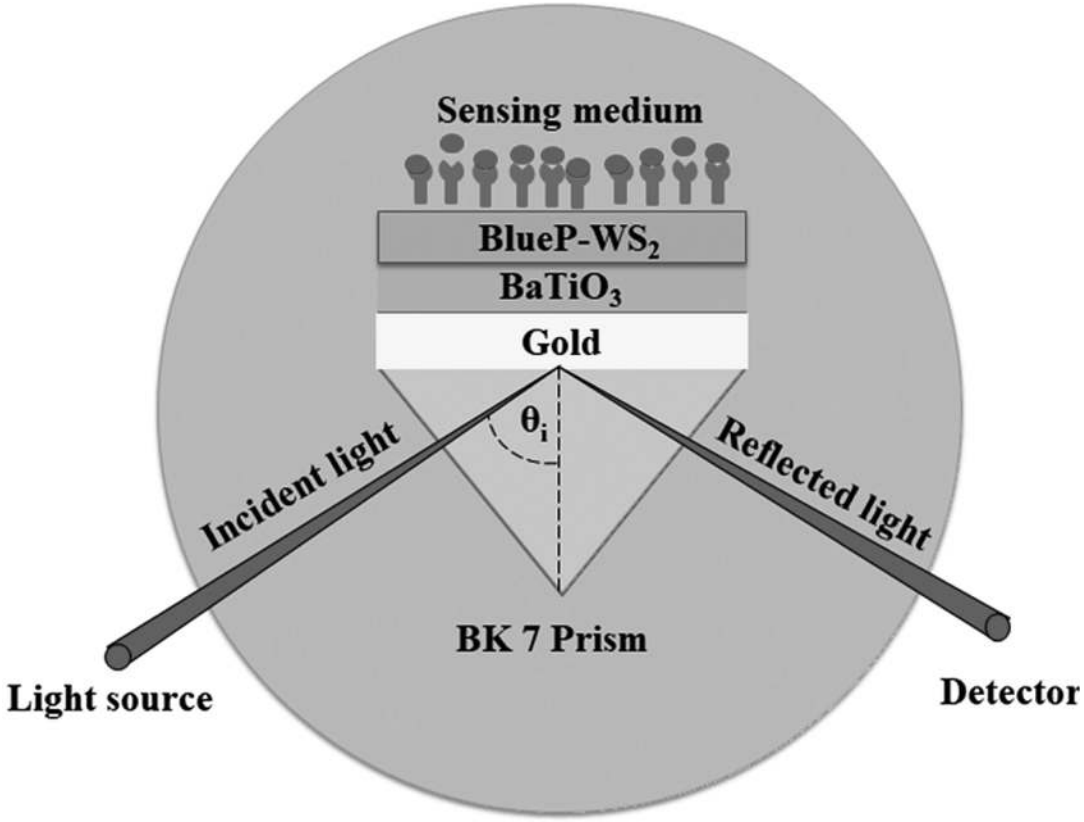

FIGURE 13.7 Schematic representation of Design III.

TABLE 13.8 Performance Measuring Parameters with Increment in BlueP-WS_2 Layers for Design III.

BlueP-WS2 Layers	Sensitivity (°/RIU)	FWHM(°)	QF (RIU^{-1})
1	218	5.5287	39.43
2	236	5.61379	42.03
3	260	5.89366	44.11
4	220	7.33395	29.99

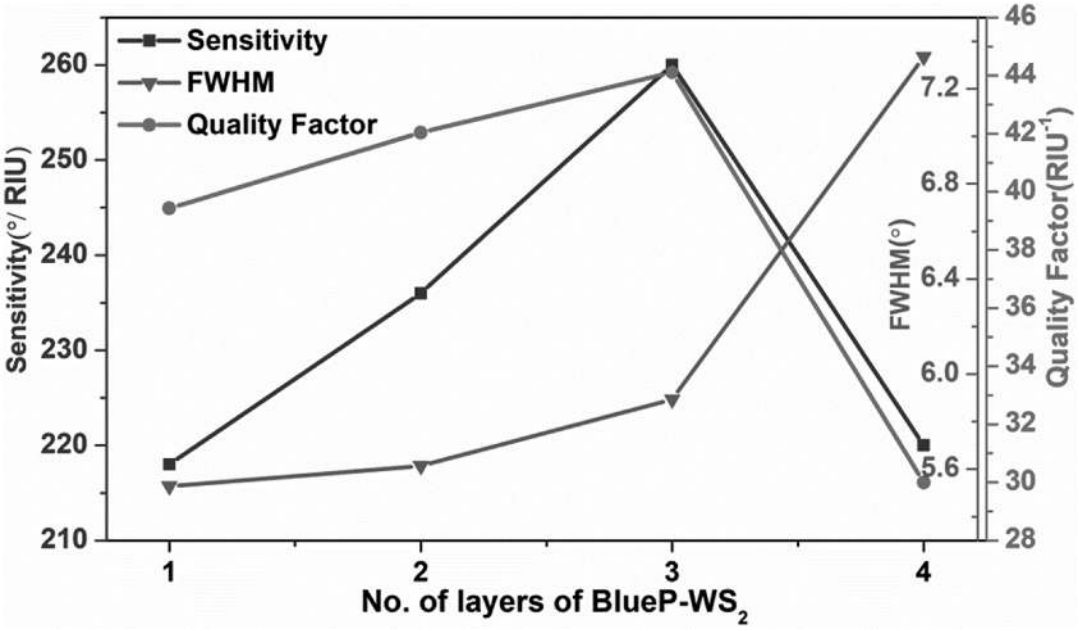

FIGURE 13.8 Change in the performance measuring parameters with increment in BlueP-WS_2 layers for Design III.

Design IV

In the proposed sensor (Design IV), BlackP nanomaterial is deposited over the BlueP-WS_2 heterostructure with optimized thicknesses of Au, $BaTiO_3$, and BlueP-WS_2 as 56, 1.6, and 2.25 nm (trilayer). The changes in performance measuring parameters with increment in BlackP layers for Design IV are shown in Table 13.9 and Figure 13.9. It is evident from the figure that seven layers of BlackP (3.71 nm) results in the highest sensitivity of 280°/RIU with FWHM and QF of 6.14812° and 45.54 RIU^{-1}, respectively.

TABLE 13.9 Performance Measuring Parameters with Increment in BlackP Layers for Design IV.

BlackP Layers	Sensitivity (°/RIU)	FWHM(°)	QF (RIU^{-1})
1	225	5.4712	41.12
2	231	5.5235	41.82
3	237	5.6321	42.08
4	240	5.7001	42.10
5	244	5.7321	42.56
6	248	5.803	42.73
7	280	6.14812	45.54
8	248	7.00568	35.39

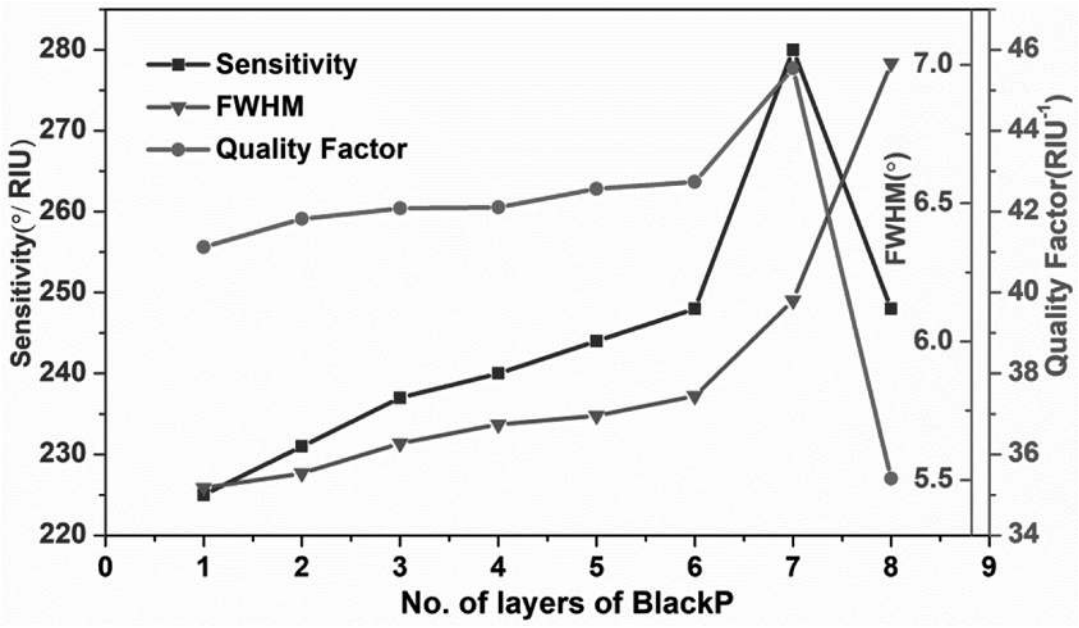

FIGURE 13.9 Change in performance measuring parameters with increment in BlackP layers for Design IV.

13.3.2 COMPARATIVE ANALYSIS

Figure 10.10 shows the schematic illustration of Design I, II, III, and IV. Table 13.10 illustrates the performance evaluation parameters of the designs for 0.005 RIU variation of RI of the sensing layer. Design I exhibits a resonance angle ($\Delta\Theta_{res}$) difference of 0.86° demonstrating sensitivity of 172°/RIU with FWHM of 4.26311° and QF of 40.35 RIU^{-1}. For Design II, BlueP-WS_2 is presented as a heterostructure layer over Au causing an increase in $\Delta\Theta_{res}$ to 1.15° resulting in improved sensitivity of 230°/RIU over Design I, with FWHM and QF of 4.86336° and 47.29 RIU^{-1}, respectively. In Design III, a layer of $BaTiO_3$ is introduced over the Au layer producing a further increase in $\Delta\Theta_{res}$ to 1.3° producing a sensitivity of 260°/RIU having FWHM of 5.89366° and QF of 44.11 RIU^{-1}. In Design IV, BlackP as a 2D nanomaterial layer is introduced over BlueP-WS_2 heterostructure, producing a total increase of $\Delta\Theta_{res}$ to 1.4° resulting in sensitivity of 280°/RIU with FWHM of 6.14812° and QF of 45.54 RIU^{-1}. Among all the designs, Design IV presents the highest sensitivity demonstrating sensitivity enhancement by 1.63, 1.21, and 1.07 times over Design I, II, and III, respectively. In addition to the improvement of

sensitivity, the proposed SPR sensor also shows an enhancement in the QF by1.13 times over Design I.

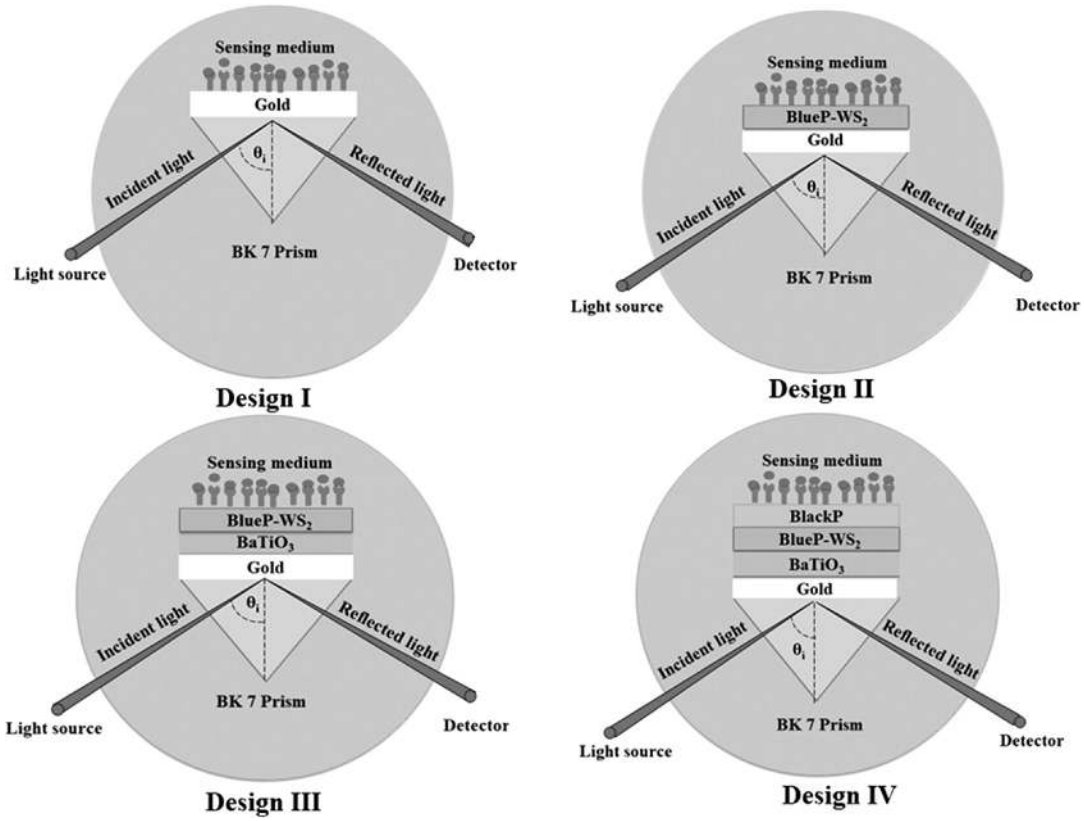

FIGURE 10.10 Schematic illustration of the SPR sensor designs.

TABLE 13.10 Comparison of the SPR Sensor Designs.

Design	RI Shift (Δn) (RIU)	Resonance Angle Change (ΔΘres) (°)	S(°/RIU)	FWHM (°)	QF (RIU^{-1})
Design I	0.005	0.86	172	4.26311	40.35
Design II	0.005	1.15	230	4.86336	47.29
Design III	0.005	1.3	260	5.89366	44.11
Design IV (Proposed)	0.005	1.4	280	6.14812	45.54

13.3.3 COMPARISON OF SENSITIVITY OF THE PROPOSED SENSOR

The sensitivities of a few SPR sensors reported recently are presented in Table 13.11 for comparison with the sensor proposed in this chapter. Table 13.11 illustrates that the proposed sensor performs better than a large number of other SPR sensors [50, 51, 52, 53, 54, 55, 56 and 57]. On the other hand, some of the reported works also demonstrate improved sensitivities than the sensor designed in this chapter due to the use of Ag and prisms with lower RI than BK7, such as CaF_2, FK51A, and so forth [58, 59, 60, 61, 62 and 63]. However, Ag oxidizes rapidly, thus compromising the stability of the sensor. Prisms having low RI deteriorate the detection accuracy of SPR sensors due to increase in the FWHM [37].

TABLE 13.11 Comparison of Sensitivity of the Designed Sensor at 633 nm Wavelength.

SPR Designs	Sensitivity(°/RIU)	References
Layer 1: SF10, Layer 2:Au, Layer 3:ZnO, Layer 4: Graphene, Layer 5: Sensing medium	156.33	[50]
Layer 1:BK7, Layer 2: ZnO, Layer 3:Ag, Layer 4:BaTiO3, Layer 5:WS_2, Layer 6:Sensing medium	180	[51]
Layer 1:BK7, Layer 2:Au, Layer 3:MXene, Layer 4: WS_2, Layer 5: BlackP, Layer 6:Sensing medium	190.22	[52]
Layer 1:BK7, Layer 2:Au, Layer 3: BlueP-MoS_2, Layer 4:Sb, Layer 5: Sensing medium	194.8	[53]
Layer 1:BK, Layer 2:Au, Layer 3:BlackP, Layer 4:Au, Layer 5:Graphene, Layer 6:Sensing medium	218	[54]
Layer 1:BK7, Layer 2:TiO_2, Layer 3:Au, Layer 4:MXene, Layer 5:Sb, Layer 6:Sensing medium	224.26	[55]
Layer 1:BK7, Layer 2:MgO, Layer 3:Ag, Layer 4:BlackP, Layer 5:Sensing medium	234	[56]

SPR Designs	Sensitivity(°/RIU)	References
Layer 1:BK7, Layer 2:ZnO, Layer 3:Au, Layer 4:BlueP-MoS_2, Layer 5:Sensing medium	260	[57]
Layer 1:BK7, Layer 2:Au, Layer 3: $BaTiO_3$, Layer 4:BlueP-WS_2, Layer 5:BlackP, Layer 6:Sensing medium	280	This chapter
Layer 1:CaF2, Layer 2:Ag, Layer 3:BlueP-MoS_2, Layer 4: MXene, Layer 5:Sensing medium	302	[58]
Layer 1:FK51A, Layer 2:Ag, Layer 3:$BaTiO_3$, Layer 4:BlueP-MoS_2, Layer 5:Sensing medium	347.8	[59]
Layer 1:BK7, Layer 2: Ag, Layer 3:Au, Layer 4: WS_2, Layer 5:MXene, Layer 6:Sensing medium	348	[60]
Layer 1:BK7, Layer 2:Ag, Layer 3:ITO, Layer 4:BlueP-WS_2, Layer 5:Graphene, Layer 6:Sensing medium	348.8	[61]
Layer 1:CaF2, Layer 2:Ag, Layer 3:Al_2O_3, Layer 4:Nickel, Layer 5: BlueP-WS_2, Layer 6:Sensing medium	374	[62]
Layer 1:BK7, Layer 2:Ag, Layer 3:BlackP, Layer 4:WS_2, Layer 5:MXene, Layer 6: Sensing medium	388	[63]

13.4 CONCLUSION

This chapter proposes an SPR sensor having enhanced sensitivity utilizing novel materials, namely $BaTiO_3$, heterostructure of BlueP-WS_2, and BlackP. The performance measuring parameters of the sensor are evaluated at a working wavelength of 633 nm for 1.33–1.335 RIU. The thicknesses of the Au, $BaTiO_3$ and different layers of BlueP-WS_2, and BlackP are tuned to yield a maximum sensitivity of 280°/RIU. The sensor (Design IV) with 56 nm Au, 1.6 nm $BaTiO_3$, trilayer of BlueP-WS_2 (2.25 nm), and seven layers of BlackP (3.71 nm) exhibits sensitivity enhancement by 1.63 times over Design I and demonstrates better sensitivity than many recently reported works. The use of promising materials, namely $BaTiO_3$,

BlueP-WS_2, and BlackP; produce high resonance shifts, thus leading to the enhanced sensitivity. The sensor proposed in this chapter is appropriate for the sensing layer for 1.330–1.335 RI range.

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KEYWORDS

- **evanescent wave**
- **heterostructure**
- **novel materials**
- **prism**
- **quality factor**
- **SPR sensitivity**
- **surface plasmon resonance**

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Index

A

Acquired immunodeficiency syndrome (AIDS), 218
AES S-boxes, 60
    hardware solutions, 61
AES subbytes transformation
    modified S-box based, 63–64
    VLSI implementation, 64–69
        blocks were merged, operator (OP) was added, 65–66
        GF (22), decreased crucial route of multiplication, 68–69
        multiplexor to construct, employing, 66–68
Amplifiers 1–2, 144, 153
Ansoft HFSS software, 41
Antenna-feeding techniques
    microstrip patch antenna, 46–47
    square microstrip patch antenna
        using square EBG structure, 47–49
        without and with EBG structure, 49–51
Autolab Potentiostsat/Galvanostat, 190

B

Binarized convolution neural network (BCNN)
    related works on, 29
        convolutional layer, 29–30
        fault injection mechanism in, 34

fully connected layer, 31
input image matrix and kernels, 32
non-faulty steps, 32
output after fault injection in, fully connected, 34
output of fully connected layer, 33
pooling layer, 30–31
rectified linear unit (ReLU), 30
simulation report, 37–38
Binarized neural network (BNN), 24
Bipolar junction transistors (BJTs), 155
Bit independent criterion (BIC), 74
Bulk MOSFETs, 6
Bulk planar junction-less transistor (BPJLT), 11

C

Cadence Virtuoso tool, 171
Cantilever
HIV detection, 218
Cascade amplifiers, 155
Cascode amplifiers, 156
Circuit-level fault injection, 27
CMOS technology, 2
Complementary metal oxide semiconductor (CMOS) technology, 101
Convolutional neural network (CNNs), 24–26

D

Darlington amplifiers, 155–156
Deep neural network (DNNs), 24–25

hidden layer, 25
input layer, 25
output layer, 25
Device-level implementation, 109–111
1-bit comparator, 110
single-bit reversible comparator, 110
DG MOSFET's
structure, 7
Digital-to-analog converter (DAC), 171
Distributed amplifiers, 156–157
Double-gate (DG) junctionless transistor, 12–13
Double-gate (DG) MOSFETs, 2–7
construction, 4
four terminal driven mode, 3–4
lack of depletion charges in, 6
leakage current, 5
multigate MOSFET structure, 9
research outline of modeling, 7–8
short channel effect, 4
structures, 3, 6
three terminal mode, 3
Drude-Lorentz model, 232
Dual-frequency slotted waveguide array antenna (DF-SWA), 85
conventional design, 88–89
enhanced design, radiated emission at S-band
frequency at S-band, 95
non-uniform aperture distribution, 92–93
performance analysis, 94–96

ridged waveguide, 92
sub-arrays, 93–94
future scope, 96–98
observations, 89–92
Dual-frequency synthetic aperture radar (DF-SAR) antenna, 85, 88
enhanced design
frequency at S-band, 95
non-uniform aperture distribution, 92–93
performance analysis, 94–96
radiated emission at S-band, 95
ridged waveguide, 92
sub-arrays, 93–94
future scope, 96–98
layout diagram of Ch-II's, 89
observations, 89–92
Dynamic fault injection, 27

E

Eigenstate, 123
Electromagnetic band gap (EBG), 42–43
Electromagnetic bandgap (EBG), 47
Environmental fault injection, 27
Enzyme linked through immunosorbent assay (ELISA), 218

F

Fault injection techniques, 26
circuit-level fault injection, 27
dynamic fault injection, 27

environmental fault injection, 27
HWIFI, 27
PFI, 27
SEU injection, 27
SWIFI, 26–27
testing tools, 27
TFI, 27
Fault injection testing tools, 27
Fault tolerance, 28
complexity of modern systems, 28
cost of downtime, 28
critical applications, 28
data integrity, 28
hardware and software imperfections, 28
reliability and availability, 28
scalability, 28
Fault-tolerant CNN
design and implementation of, 23–38
BCNN, 29–34
DNNs, 24–35
injection techniques, 26–27
simulation report, 37–38
tolerance, 28
Xilinx FPGA Artex7, 35–37
Fermi-Dirac distribution function, 124
Fermi's golden rule, 124, 130
Feynman reversible gate, 107–109
QCA, implementation of, 108

simulation result, 108–109
FinFETs, 6
Flexible slotted waveguide antenna array (SWAAs)
benefits over microstrip arrays, 87–88
layout and performance
DF-SAR antenna, Ch-II, 88
DF-SWA antenna, 88–89
Fourier transform infrared spectroscopy (FTIR), 197
Fredkin reversible gate, 105–107
QCA, implementation of, 106
simulation result, 107
Fully depleted silicon on insulator (FDSOI) technology, 9

G

Graphene, 184
electrochemical measurement, 191–197
structure, 187
thin film deposition, 189–190
Graphene oxide (GO), 184
cyclic voltammogram (CV) curve, 192
doping, 186–189
electrical equivalent circuit for, 193
electrochemical measurement, 191–197
element analysis, 204–205
FTIR spectroscopy, 197–199
preparation, 185–186
Raman spectroscopy analysis, 200–202
SEM analysis, 202–204

structure, 187
thin film deposition, 189–190
XRD analysis, 199–200

H

Hardware-based fault injection (HWIFI), 27
Heterojunction solar cells (HJSCs), 210
application of ZnO-SnO2 in, 210
effect of work function on cell parameters, 209–222
displacement with square diaphragm, 222
open circuit voltage, 213
power consumption efficiency, 214
results and discussion, 212–215
modeling and simulation, 210–212
High-gain multistage CMOS amplifiers
affecting factors, 159
device parameters and characteristics, 159
frequency-dependent gain, 160
load and source impedances, 160
parasitic effects, 161
power supply variations, 160–161
bandwidth, 147
challenge of designing, 147–149
bandwidth limitations, 149
noise considerations, 148
power consumption, 149
stability and compensation, 148
design at 45-nm technology node, 149–150

bandwidth enhancement strategies, 151
with noise optimization, 150
outcomes of DC and transient analysis, 152
power optimization, 151–152
stability enhancement and compensation techniques, 151
improved significance, 146
power consumption, 147
simulation results, 152
amplifier 1, for, 153
amplifier 2, for, 153
comparative analysis, 153–154
verification against design specifications, 154
trade-offs between performance metrics, 162
bandwidth *versus* noise gain, 162–163
gain-bandwidth trade-off, 163
gain *versus* noise figure, 162
power consumption *versus* gain, 163
transconductance of transistor, 147
types, 154–155
cascade, 155
cascode, 156–157
Darlington, 155–156
distributed, 156–157
operational amplifiers (op-amps), 157–158
use to achieve high gain, 144–145
High pass filter (HPF), 171, 176–177
characteristics, 177
circuit diagram, 177

I

Immunodeficiency virus (HIV), 218
Internet of Things (IoT), 55–56
    comparative analysis of execution time, 70–71
        nine irreducible polynomial, 71
        over traditional S-box and random S-box, 76–77
        security analysis, 71
    complexity analysis
        brute force cryptanalysis, 78
        time, 78
    hardware (VLSI) S-box implementation, 78–80
    modified S-box based AES architecture in, 63
        hardware architecture, 63–64
        software algorithm, 69–70
        VLSI implementation, 64–69
    security analysis, 71
    bit independent criterion (BIC), 74
    differential computation (DP) probability, 75–76
    linear approximation probability, 74–75
    nonlinearity, 72–73
    strict avalanche criteria (SAC), 73–74

J

Junctionless field-effect transistor (JLFET), 12–15
Junctionless nanowire transistor (JNT), 13–14, 15
Junctionless SOI-FET, 10
    structure, 11
Junctionless transistors (JLTs), 10

JLFET, 14–15
JNT, 13–14, 15
structural classification, 10, 13
bulk planar, 11
double gate, 12–13
Junctionless trigate structure, 13

K

Klein-Gordon equation, 126
Kronecker delta function, 129

L

Linear approximation probability, 74–75
Logic-level implementation, 111–114
proposed single-bit reversible comparator
logic-level implementation, 113
RTL schematic, 113
simulation result of, 112, 114
Long silicon channels, 6–7
Lorentzian line shape function, 129
Low pass filter (LPF), 171, 176–177
characteristics, 176
circuit diagram, 176

M

Majority voter (MV), 103–105
Memristor, 169
categories, 170

fundamental attribute, 170
Memristor-based 2 × 1 multiplexer
2-bit DAC cell using two memristors, 178–179
implementation, 177–178
input and output waveform, 179
simulation results of 2-bit DAC cell, 180
Micro cantilever-based biosensor, 219
HIV detection
deflection after exposing, 222–223
displacement with square diaphragm, 222
material properties of, 220
probe coating, 219
result and discussion, 220–222
mechanism of application principle, 219
Micro-cantilever sensors, 218
Microstrip antenna, 43
microstrip line, 44
rectangular microstrip patch antenna, 45–46
surface wave effect, 43
Microstrip line, 44
Microstrip patch antenna, 46–47
with EBG structure
characteristic impedance, 51
characteristic impedance of, 51
return loss, 49–50
without EBG structure
gain output, 51
without EBG structure.

characteristic impedance of, 52
Microwave remote sensing, 85
MOSFET-based memristor, 169
applications
2-bit DAC cell using two memristors, 178–179
implementation of 2 × 1 multiplexer, 177–178
LPF and HPF, 176–177
description and analysis, 171–173
simulation results, 173–175
hysteresis graph, 175
hysteresis loop, 174
transient analysis, 174
Multiple-input multiple-output (MIMO) systems, 42
Multistage CMOS amplifiers, 144
architecture, 143

N

Nanoelectronic devices, 122
compared with electronic devices, 122
Neuro-Bit, 171
Nikiforov-Uvarov method, 126
Nucleic act test (NAT), 218
Nyquist plot, 192–193
PEI doped GO of, 194
rGO and PEI doped rGO, 196

O

Operational amplifiers (op-amps), 157–158

Operational transconductance amplifier (OTA), 144
Oscillator strength
contact barrier widths, 137, 138
triangular quantum well structure, fluctuation for, 137
well widths, 137

P

Perfect of Q, 60
Permanent fault injection (PFI), 27
PGSTAT128N system, 190
Plasmon, 230
Polyaniline (PANI), 184
Polyethylenimine (PEI) polymer, 185, 186
cyclic voltammogram (CV) curve, 192
electrochemical measurement, 191–197
element analysis, 204–205
FTIR spectroscopy, 197–199
Raman spectroscopy analysis, 200–202
SEM analysis, 202–204
structure, 189
thin film deposition, 189–190
XRD analysis, 199–200
Polyurethane acrylate (PUA), 184

Q

QCADesigner, 104–105
simulation parameters, 105
Quantum confinement, 122

Quantum-dot cellular automata (QCA), 101–103
comparative analysis, 117
defect analysis, 114–116
implementation of Feynman gate, 108
implementation of Fredkin gate, 106
parameters analysis, 117
proposed single-bit reversible comparator, 111
Quantum well
absorption coefficient for, 124
eigenstates and intersubband *transition in, 123
importance of triangular, 124–126

R

Rectangular microstrip patch antenna, 45–46
Reduced graphene oxide (rGO), 184
CV curves, 195
doping, 186–189
electrical equivalent circuit for, 196
electrochemical measurement, 191–197
element analysis, 204–205
FTIR spectroscopy, 197–199
preparation, 185–186
Raman spectroscopy analysis, 200–202
SEM analysis, 202–204
structure, 188
thin film deposition, 189–190
XRD analysis, 199–200
Remote sensing, 85–86

Reversible circuits, 103

S

S-box, 57–58
4-bit, 62
composite field arithmetic, 58–59
Galois field GF(28), 59–60
lightweight design, 62
substitution box conversion, 58
Schrödinger equation, 122, 125
time-independent, 127–129
Short channel effect, 4
Silicon
material properties of, 220
Single event upset (SEU) injection, 27
Software-based fault injection (SWIFI), 26–27
Square microstrip patch antenna
electromagnetic bandgap structure incorporated, impact, 41
using square EBG structure, 47–49
without and with EBG structure, 49–51
Strict avalanche criteria (SAC), 73–74
Surface plasmon (SPs), 230
electromagnetic field, 231
excitation, 231
Surface plasmon resonance (SPR), 228
2D nanomaterials, 228
Kretschmann angular interrogation mode, 228
layer arrangement, 233

materials selected, 233–234
2D nanomaterial layer, 235
glass prism, 234
heterostructure layer, 234
light source, 235
metal layer, 234
oxide layer, 234
sensing layer, 235
optical fibers limitations, 228
performance evaluating parameters, 235–236
proposed sensor, comparison of sensitivity, 243
SPR sensor designs, 243
results and discussion
comparative analysis, 240–242
optimization of thickness, 236–240
RI
glass prisms used in, 230
metal oxides used in, 229
single layer thickness of heterostructures, and 2D nanomaterials, 229
sensitivity improved sensor, design, 227–245
sensor theory and mathematical modeling, 230–233
usage, 228
Surface plasmon wave (SPW), 230
propagation constant, 230
Surface wave effect, 43

T

Transfer matrix method (TMM)., 227
Transient fault injection (TFI), 27
Transmission coefficient
function of energy, as
contact barrier widths in presence of bias, 133
material compositions in presence of bias, 134
middle barrier widths in presence of bias, 133
function of energy, as
presence and absence of bias in, 131
function of energy, as
widths in presence of bias, 132
variation of absorption
different barrier widths for, 135
different well widths for, 135
middle barrier widths for, 136
Triangular quantum well, 124–126
molecular spectroscopy, in, 125
Tri-gate MOSFETs, 6–7

V

Very large scale integration (VLSI), 55–56

W

Wireless communication systems, 42

X

Xilinx FPGA Artex7, 35
design implementation using, 35–37

device utilization summary, 36
HDL synthesis report, 37

Z

Zinc oxide (ZnO), 210