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Reliability of CMOS Analog ICs

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Preface

The use of statistical approach for reliable and optimal design of systems, including electronic systems, has become quite popular. Statistically designed experiments/ simulations have been used extensively for estimating or demonstrating existing reliability by identifying the important parameters (factors) affecting reliability out of many potentially important ones. This statistical approach ensures the performance and safety of critical electronic systems employed in space, nuclear, automotive, defence industry, submarine, and aerospace applications, to name a few.

In most reliability studies on modeling the hot-carrier effect available in the literature, models based on physical properties have been proposed; however, difficulties in preparation of physical models, losing the actuality within the advances in the technology, and excessively long simulation times seem to be disadvantages of these models.

To overcome these disadvantages of physical models, statistical methods based on the observation results, independent of the technology, and exhibiting a short simulation time and high accuracy have been introduced in our work.

Although digital signal processing is becoming increasingly more powerful and many types of signal processing have indeed moved to digital domain due to the advances in IC technology, analog circuits are fundamentally necessary in many complex and high performance systems. This is caused by the fact that naturally occurring signals are analog. In other words, analog circuits act as a bridge between the real world and digital systems. In analog signal processing, many circuit topologies including active filters, oscillators, immittance simulators, etc. have been proposed in the literature. Application area of analog signal processing is wide and ranges from very low frequencies at several Hz levels to RF applications operating at GHz level, which means from biomedical and sonar signals to cognitive radio and encrypted communications. Today, modern CMOS technologies are continuously scaling down; but as a result of this, analog designers have serious reliability problems in their designs caused by physical effects.

This book gives a review of our previously performed and published works in the open literature on statistical method-based modeling of the experimental studies on degradation in the drain current and threshold voltage of the NMOS and PMOS

transistors, including power MOSFETs. All these works were performed by our research group in the frame of Ph.D. and M.Sc. thesis works in Istanbul University and Istanbul Technical University. Note that these models are based on the observations by operating the device under stress voltage conditions.

We believe that this book will be useful for analog circuit designers working in the related area and provides a simple and useful alternative to physical methods available in the literature.

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Dedication to Ayten Kuntman

In loving memory of Prof. Dr. Ayten Kuntman (1956–2023)

We started actually with Prof. Dr. Ayten Kuntman to prepare this book, where she was one of the authors of the works performed; unfortunately, we lost Prof. Kuntman in 2023. We continued with other colleagues, two are her former Ph.D. and M.Sc. students in the research group; they are also coauthors of these works.

We always remember her name and her contribution to this book.

Istanbul, Turkey — Hakan Kuntman

Contents

About the Author

Hakan Kuntman received his B.Sc., M.Sc., and Ph.D. degrees from Istanbul Technical University in 1974, 1977, and 1982, respectively. In 1974, he joined the Electronics and Communication Engineering Department of Istanbul Technical University. Since 1993, he has been a Professor of electronics in the same department, from which he retired in 2016. His research interest includes the design of electronic circuits, modeling of electron devices and electronic systems, active filters, and the design of analog IC topologies. Dr. Kuntman has authored many publications on modeling and simulation of electron devices and electronic circuits for computer-aided design, analog VLSI design, and active circuit design. He is the author or co-author of 129 journal papers published or accepted for publishing in international journals, 179 conference papers presented or accepted for presentation in international conferences, and 161 Turkish conference papers presented at national conferences. Additionally, he has written 10 books related to the above-mentioned areas, with an h-index of 39. He has advised and supervised the completion of the work of 16 Ph.D. and 44 M.Sc. students. Dr. Kuntman is a member of the Chamber of Turkish Electrical Engineers (EMO).

From 2001 to 2004, he served as the Head of the Electronics and Communication Engineering Department, and from 2004 to 2010, he was the Dean of the Electrical and Electronics Engineering Faculty at Istanbul Technical University. Furthermore, Dr. Kuntman is one of the founders of the ELECO conferences and acted as the Conference Chairman several times. His book entitled *Trends in Circuit Design for Analog Signal Processing* was published by Springer in 2022.

Deniz Özenli received his B.Sc. degree in Electrical and Electronics Engineering from Istanbul University in 2009 and his M.Sc. and Ph.D. degrees from Istanbul Technical University in 2011 and 2018, respectively. During his Ph.D., he carried out different analog filter applications based on MOSFET-only and MOSFET-C building blocks. He is now an Associate Professor in the Electronics Engineering department of the Turkish Air Force Academy. His main research interests include analog filters, low-voltage current and voltage mode circuits, computer-aided ana-

log circuit design, VLSI design, as well as image and video processing. He is the author or co-author of approximately 38 scientific papers published in well-esteemed journals and conference proceedings.

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Yasin Özçelep received his B.Sc., M.Sc., and Ph.D. degrees in Electrical and Electronics Engineering from Istanbul University in 2002, 2004, and 2009, respectively. He is currently a Full Professor at the Electrical and Electronics Engineering Department of Istanbul University-Cerrahpasa. His current research interests include semiconductor devices, micro-nano electronics, reliability modelling of semiconductor devices, and hydrogen fuel cells. During his tenure as a faculty member, he has supervised and completed the supervision two Ph.D. and four M.Sc. theses. He has worked as a manager or researcher on 13 research projects. He is the author or co-author of approximately 41 papers published in scientific journals or conference proceedings. He currently serves as the vice-chair of the Department of Electrical and Electronics Engineering at Istanbul University-Cerrahpasa.

Chapter 1
Introduction

The down-scaling of device dimensions in MOS technology will improve performance and packing density for VLSI circuits, but it will negatively affect the quality of the circuits because of reliability problems arising from several physical degradation effects.

Although digital signal processing is becoming increasingly more powerful and many types of signal processing have indeed moved to digital domain due to the advances in IC technology, analog circuits are fundamentally necessary in many complex and high performance systems. This is caused by the reality that naturally occurring signals are analog. In other words, analog circuits act as a bridge between the real world and digital systems. In analog signal processing, many circuit topologies including active filters, oscillators, immittance simulators, etc. have been proposed in the literature [1–22].

Application area of analog signal processing is wide and ranges from very low frequencies at several Hertz levels to RF applications operating at gigahertz level, that means, from biomedical and sonar signals to cognitive radio and encrypted communications [1, 2, 11, 12, 14–17, 20–22].

Today, modern CMOS technologies are continuously scaling down; but as a result of this, analog designers have serious reliability problems in their designs caused by physical effects such as

– Hot-carrier injection,
– negative and positive bias temperature instability (N/PBTI),
– time-dependent dielectric breakdown (TDDB) [23–58].

Therefore, it is an important factor estimating the deviations caused by these degradation mechanisms to obtain a robust design. Note that the reliability of CMOS structures are considered for more than 40 years [58–64]. The subject is still popular and several new publications are available in the literature [49–54, 63].

The reliability of a system is defined as the probability that it will perform its required function under stated conditions for a stated period of time.

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In most reliability studies on the modeling of the hot-carrier effect available in the literature, models based on physical properties have been proposed [23–31, 49–54]; however, difficulties in preparation of physical models, losing the actuality within the advances in the technology, and excessively long simulation times seem to be disadvantages of these models.

To overcome these disadvantages of physical models, statistical methods based on the observation results, independent of the technology, and exhibit a short simulation time and high accuracy has been introduced in our work.

The use of statistical approach for reliable and optimal design of systems, including electronic systems, has become quite popular. Statistically designed experiments/simulations have been used extensively for estimating or demonstrating existing reliability by identifying the important parameters (factors) affecting reliability out of many potentially important ones [1, 2]. This statistical approach ensures the performance and safety of critical electronic systems employed for space, nuclear, automotive, weapons, sub-marine and aerospace applications, to name a few [60, 61, 64]. A statistical life model becomes more reliable, valuable, and useful, if it fits the experimental data quite well.

Starting with experimental results of Siemens AG., Munich, Germany [35] and TUBITAK (Turkish Research and Technological Council), the effect of hot carriers on the drain current and threshold voltage of PMOS and NMOS transistors was statistically investigated and a statistical model was proposed as an alternative to those available in the literature [32–34, 43–48].

This book gives a review of our previously performed works on statistical method based modeling of the degradation in the drain current and threshold voltage of the NMOS and PMOS transistors. All of the works were performed by our research group in the frame of Ph.D. and M.Sc. Thesis works in Istanbul University and Istanbul Technical University [32–34, 43–48]. Note that these models are based on the observations by operating the device under stress voltage conditions.

For this purpose, measurements are performed on test transistors fabricated with the same technology but with different channel lengths. In other words, to specify the model, test transistors with different dimensions are necessary. Note that these measurements and observations are also needed for physical modeling, but complex equations must be derived for this purpose and implemented into circuit simulators which appear as an important disadvantage [35, 36].

The time-dependent statements of degradation were obtained by using different statistical methods. Coefficients were optimized with these methods and functions were generated. These functions gave variations of drain current with time and channel length. The observed and the estimated values of the degradation are compared.

The structure of the book is as follows: The Introduction Section, Chap. 1, describing the basic concept is followed by Chap. 2 reflecting the definition of reliability analysis and statistical methods. The reliability model for PMOS and NMOS transistors based on statistical methods are given in this section. Demonstration on interesting application examples are given in Chap. 3 which reflects the behavior of a current source-loaded single stage amplifier, CMOS inverter and CMOS OTA. The

following part, Chap. 4, describes in detail the behavior of a CMOS OTA operating in subthreshold region which is also demonstrated with measurement results. Two different methods are given in this chapter. In addition, a CMOS degradation macromodel is also introduced in this section. Finally, Chap. 5 describes the reliability of power MOSFET circuits demonstrated by giving example circuits.

We think that this book will be useful for analog circuit designer working in the related area and provides a simple and useful alternative to physical methods available in the literature.

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Chapter 2
The Reliability Model for PMOS and NMOS Transistors Based on Statistical Methods

Basic Concepts: Reliability and Lifetime Definitions

The use of statistical approach for reliable and optimal design of systems, including electronic systems, has become quite popular [1–42]. Statistically designed experiments/simulations have been used extensively for estimating or demonstrating existing reliability by identifying the important parameters (factors) affecting reliability out of many potentially important ones [1, 2]. This statistical approach ensures the performance and safety of critical electronic systems employed for space, nuclear, automotive, weapons, sub-marine, and aerospace applications, to name a few [40–42]. A statistical life model becomes more reliable, valuable and useful, if it fits the experimental data quite well.

In this section, we begin with the definition of the basic concept of reliability and lifetime estimation concepts. The reliability of a system is defined as the probability that it will perform its required function under stated conditions for a stated period of time.

In most reliability studies on the modeling of the hot-carrier effect available in the literature, models based on physical properties have been proposed [1–8, 27–32]; however, difficulties in the preparation of physical models, losing the actuality within the advances in the technology, and excessively long simulation times seem to be disadvantages of these models.

In order to allow a prediction of device lifetime in real life, stress levels from results obtained under actual stress conditions must be used. With such results, empirical models for hot-carrier degradation and several extrapolation laws to calculate the lifetime have been developed. However, the proposed model combines a hot-carrier degradation model and lifetime prediction model into a single model [3–7]. Lifetime predictions for MOS transistors have been performed using the criteria given in the literature [3]. They can reach 10% of the lifetime criteria [3] for hot carriers in DC stress applications in 10 years or less.

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Table 2.1 Obtained functions of the investigated methods [3]

Power method	$F(t) = a \cdot t^b$
Power-log-I method	$F(t) = a \cdot \ln(t)^b$
Power-log-II method	$F(t) = a \cdot t^b \cdot \ln(t)$
Weibull method	$F(t) = 1 - \exp[-(t/a)^b]$

Table 2.1 tabulates obtained functions of the investigated methods where for all methods t = time, a = scale parameter, b = shape parameter. Calculations are based on linear regression method for the four approaches and least squares methods have been used [10, 21, 24, 25]. So, calculations were performed by using MATLAB program.

Statistical Analysis

Life models establish a relationship between applied stresses and failure time. They provide useful parameters for material characterization and comparison [6]. Several authors proposed probabilistic life models for insulating materials subjected to electrical and thermal stresses. In general, these models are derived from two basic approaches. One model is based on the study of degradation breakdown mechanisms and provides as a final product a relationship between applied stresses and time to breakdown. The other model deals with the phenomenological observations of the results of life tests and tries to fit these results to appropriate models. In both cases, however, the problem to individualize the behavior of an insulating material subjected to selected stresses, based on the results of life tests, is quite difficult due to the hidden technological features, such as curing technique, test cell, test methods, and other factors [7]. A statistical life model becomes more reliable, valuable, and useful, if it fits the experimental data quite well.

Since the 1970s, the Weibull probability distribution has gained wide acceptance in the statistical treatment of the time to electrical breakdown of solid dielectrics. It affords an excellent approximation to the probability law of many random variables. Many methods, such as "maximum likelihood," "linear estimation" or "graphical plotting technique," have been developed to estimate the parameters. "Maximum likelihood technique" is the best method among them, because it can be used for any number of test specimens and can estimate the parameters quite accurately. "Linear estimation" methods are also quite accurate; however, they require extensive tables of factors for each sample size [8, 9, 15].

The "graphic plotting technique" has the disadvantage in being an observer. The data is dependent method which can lead to some inaccuracies in data statistically. However, this method is selected here because it is simple, quite easy to implement and can quickly check the validity of the Weibull distribution in representing the data [9].

The Reliability Model for MOS Transistors Based on Statistical Method

For more than 20 years, continuous scaling of CMOS devices to smaller dimensions has resulted higher devices density, faster circuit speed, and lower power dissipation. Currently, CMOS technologies less than 0.1 μm are widely used in the manufacturing of integrated circuit, several publications on analog CMOS structure and on the reliability of them are available in the literature [1–42]. Many new physical effects become significant as the device size shrinks. Examples are the drain induced barrier lowering (DIBL) [4], channel length modulation (CLM) [5], and hot-carrier effects [6–9].

Several works were performed to model the effect of hot carriers [1–42]. Some of these works are based on physical parameters [8] and the other works are focused on determination of behavior characteristics with physical quantities [6]. Both of two models are complex and take a long computational time. Parameters are characterized with respect to observation result in our studies [10, 11]. To overcome these disadvantages of the physical models, a statistical method that is based on the observation results, independent from the technology and exhibits short simulation times and high accuracy has been introduced in this work. Starting from experimental results of Siemens AG., Muenchen, Germany [13, 14], the effect of hot carriers on the drain current and threshold voltage of NMOS transistors were investigated statistically and a statistical model was proposed to be an alternative to those available in the literature. The time-dependent equations of degradation were obtained by using four different statistical methods. Due to dependence on time and channel length of obtained functions and expressions for different channel lengths with unique function supply facility in working for users obtained results can be applied to all transistors that are proposed with same process. The use of statistical approach for reliable and optimal design of systems, including electronic systems, has become quite popular. Statistically designed experiments/simulations have been used extensively for estimating or demonstrating existing reliability by identifying the important parameters (factors) affecting reliability out of many potentially important ones. This statistical approach ensures the performance and safety of critical electronic systems employed for space, nuclear, automotive, weapons, sub-marine, and aerospace applications, to name a few.

In this section, degradation models for NMOS and PMOS transistors based on statistical methods will be described. The study was performed for three different transistors produced with the same technology, but with different channel lengths [10, 21, 24, 25, 40–42]. Calculations are based on linear regression method for the four approaches and least squares methods have been used [10, 21, 24, 25]. So, calculations were performed by using MATLAB program.

It is apparent from experimental results on test transistors that the drain current and the threshold voltage of NMOS transistors decrease with time. On the other hand, experimental results also show that the drain current and the threshold voltage of PMOS transistors increases with time. The changes in the threshold voltage and

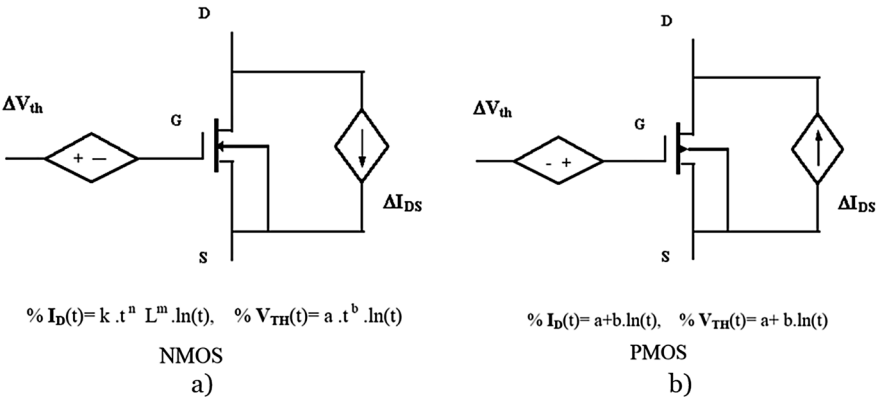

Fig. 2.1 Degradation models for NMOS and PMOS transistors [21]

in the drain current are represented by connecting a time-dependent voltage source series to the gate and a time-dependent current source parallel to drain-source terminals. According to the observed device behavior, these sources are filled with adequate statistical expressions. The related reliability models for NMOS and PMOS transistors are illustrated in Fig. 2.1a, b.

In this section, we describe the related reliability models for PMOS and NMOS transistors in detail using experimental data to demonstrate the accuracy of the method. In the first part, the statistical model for PMOS transistors is given. Second part describes the statistical model for NMOS transistors. Note that there are different mechanisms causing the degradation in PMOS and NMOS transistors.

Statistical Model of Hot-Carrier Degradation and Lifetime Prediction for PMOS Transistors

The down-scaling of device dimensions in MOS technology will improve performance and packing density for VLSI circuits, but will negatively affect the quality of the circuits. Basically, integrated circuits are classified according to the electrical function they perform. The concept of quality is used to express how well the required function is performed. Several works have been conducted on hot-carrier effect, which is one of the most important factors that influence the reliability of MOS structures [1–13]. The reliability of a system is defined as the probability that it will perform its required function under stated conditions for a stated period of time. In most reliability studies on the modeling of the hot-carrier effect available in the literature, models based on physical properties have been proposed [1–8, 13]; however, difficulties in preparation of physical models, losing the actuality within the advances in the technology, and excessively long simulation times seem to be disadvantages of these models.

To overcome these disadvantages of physical models, a statistical method that is based on the observation results, independent of the technology, and that exhibits a short simulation time and high accuracy has been introduced in this work. Starting with experimental results of Siemens AG., Munich, Germany [13], the effect of hot carriers on the drain current and threshold voltage of PMOS transistors was statistically investigated and a statistical model was proposed as an alternative to those available in the literature. The time-dependent statements of degradation were obtained by using three different statistical methods. Coefficients were optimized with these methods and functions were generated. These functions gave variations of drain current with time and channel length. The proposed method is based on the measurement results, is independent of the technology, and can be easily applied to PMOS transistors with different dimensions.

PMOS Degradation

PMOS degradation occurs only if electrons are trapped in the gate oxide due to the impact ionization of hot-holes [1–9]. This is known as the drain avalanche hot-carrier mechanism and is shown in Fig. 2.2. When the PMOS transistor is operating in the saturation region, holes move from the source to the drain and are accelerated by the high electric field at the drain end of the channel. If a hole has energy of at least 1.5 eV, then it can be concluded with impact ionization. After impact ionization, the rise of the new hole moves to the drain, as do the other holes, and it increases the drain current (I_D) a small amount. Most of the new electrons, after impact ionization, move to the substrate, forming the substrate current (I_B). Nevertheless, some of these electrons, if they have an energy at least of 3.1 eV and the right direction, they surmount the Si–SiO_2 potential barrier and are injected into the gate oxide. The electric field strength direction in the gate oxide above the depletion region causes

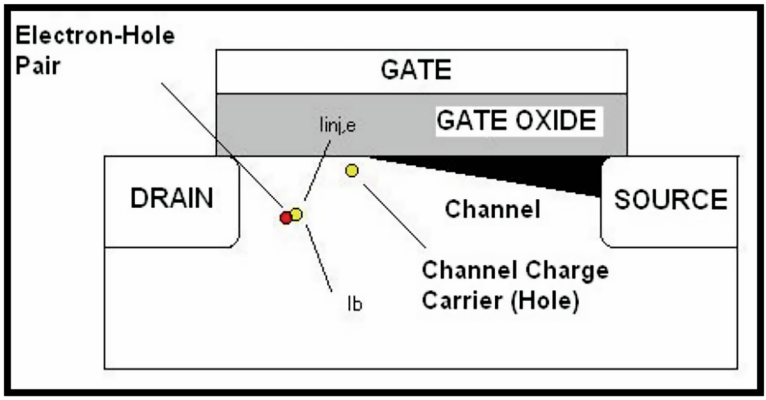

Fig. 2.2 Hot-carrier formation mechanism of PMOS transistors [21]

the electron to accelerate to the gate. Most of the electrons in the gate oxide reach the gate from the gate current (I_G), which corresponds greatly with the drain current (I_D). Yet, the existing traps in the oxide can capture some of the electrons, and these captured electrons behave like fixed negative charges. Electrons that are injected into the gate oxide can damage the Si–SiO_2 interface. These interface defects are partially filled by the holes in the non-saturation operation. Therefore, this degradation effect on a MOSFET will be ignored. The fixed negative charges of the captured electrons cause an increase in the drain current in all regions of operation; however, the largest degradation will be in the saturation operation. For short channel MOSFETs, the threshold voltage (V_{th}) will also change to lower values.

Statistical Methods

This study was performed for three different transistors produced with the same technology but with different channel lengths. Process parameters of the transistors are given as: t_{ox} = 20 nm and x_j = 400 nm; the dimensions are W = 10 μm and L = 1.5 μm, 2 μm, and 3 μm. Stress voltage was applied to the transistors for 16 h. Statistical methods were applied and investigated using variations of the drain currents and threshold voltages with time, which were obtained as a result of applied stress voltages (V_D = 0.5 V, V_D = 2.5 V, V_G = 1.5 V, V_G = 2 V, and V_G = 2.5 V). The investigated methods for PMOS transistors are:

– power method,
– Weibull method,
– logarithmic method.

Calculations were based on the linear regression method for all three approaches and the least squares method was used [21–25, 39]. Exponential and logarithmic parameters and power distribution with the least squares method are given by the following equations. Calculations were performed using the MATLAB program.

In this respect, exponential distribution with the least squares method is given as:

$$y = A\mathrm{e}^{Bx} \tag{2.1a}$$

$$a = \frac{\sum_{i=1}^{n} \ln y_i \sum_{i=1}^{n} x_i^2 - \sum_{i=1}^{n} x_i \sum_{i=1}^{n} \left(x_i \ln y_i\right)}{n\sum_{i=1}^{n} x_i^2 - \left(\sum_{i=1}^{n} x_i\right)^2} \tag{2.1b}$$

$$b = \frac{n\sum_{i=1}^{n} x_i \ln y_i - \sum_{i=1}^{n} x_i \sum_{i=1}^{n} \ln y_i}{n\sum_{i=1}^{n} x_i^2 - \left(\sum_{i=1}^{n} x_i\right)^2} \tag{2.1c}$$

where $B \equiv b$ and $A \equiv \exp(a)$.

Logarithmic Distribution with the Least Squares Method is described as follows:

$$y = a + b\ln\left(x\right) \tag{2.2a}$$

$$a = \frac{\sum_{i=1}^{n} y_i - b\sum_{i=1}^{n} \ln x_i}{n} \tag{2.2b}$$

$$b = \frac{n\sum_{i=1}^{n}\left(y_i \ln x_i\right) - \sum_{i=1}^{n} y_i \sum_{i=1}^{n} \ln x_i}{n\sum_{i=1}^{n}\left(\ln x_i\right)^2 - \left(\sum_{i=1}^{n} \ln x_i\right)^2} \tag{2.2c}$$

Power Distribution with the Least Squares Method is given as:

$$y = A\mathrm{e}^{Bx} \tag{2.3a}$$

$$a = \frac{\sum_{i=1}^{n} y_i - b\sum_{i=1}^{n} \ln x_i}{n} \tag{2.3b}$$

$$b = \frac{n\sum_{i=1}^{n}\left(\ln y_i \ln x_i\right) - \sum_{i=1}^{n} \ln x_i \sum_{i=1}^{n} \ln y_i}{n\sum_{i=1}^{n}\left(\ln x_i\right)^2 - \left(\sum_{i=1}^{n} \ln x_i\right)^2} \tag{2.3c}$$

where $B \equiv b$ and $A \equiv \exp(a)$.

Numerical Results

Experimental results for PMOS transistors at different stress conditions are summarized in the 3-dimensional plots of $I_D = I_D(L,t)$ shown in Fig. 2.3. As can be observed from Fig. 2.3, drain current increases with stress time and I_D decreases with channel length. On the other hand, based on a previous study [12], it can be easily observed that the drain current and the threshold voltage of NMOS transistors decrease with time. For $L = 1.5$ μm, the change in the drain current is approximately 4% for PMOS, while it is 0.8% for NMOS. It seems that PMOS transistors are more affected by hot carriers. The power, logarithmic, and Weibull parameters were calculated using experimental data and the linear regression method, including Equations. The functions obtained by using the investigated methods that gave the percentage changes in drain currents and threshold voltages are given in Table 2.2. Coefficients were optimized with these methods and functions were generated.

These functions gave variation of drain current with time and channel length. The function coefficients for different operating conditions obtained by the three methods can be seen in Table 2.3.

The results calculated from the equations given in Table 2.1 are compared with experimental results. It has been observed that the logarithmic method seems to be the best statistical method that characterizes the measurement results. The characterization results using the logarithmic method are given with experimental results shown in Figs. 2.4, 2.5, and 2.6.

It seems from the figures that there is good agreement between the experimental results and the calculated values. To show the similarity between the measured and calculated values, correlation coefficients were calculated and very highly correlated coefficients were obtained. The results obtained can be seen in Table 2.4. Moreover, error calculations were achieved with the RMS method and the results are given in Table 2.5. It can easily be observed that the error values are very low. With respect to the graphics, the table of correlation coefficients, and the table of RMS errors, the methods are classified from the best to worst as the logarithmic, power, and Weibull methods, respectively.

Proposed PMOS Model

It is clearly seen that the drain current and the threshold voltage of the PMOS transistor increase with time. An appropriate model was designed to represent the hot-carrier effect of the transistors in this work. With the help of the obtained

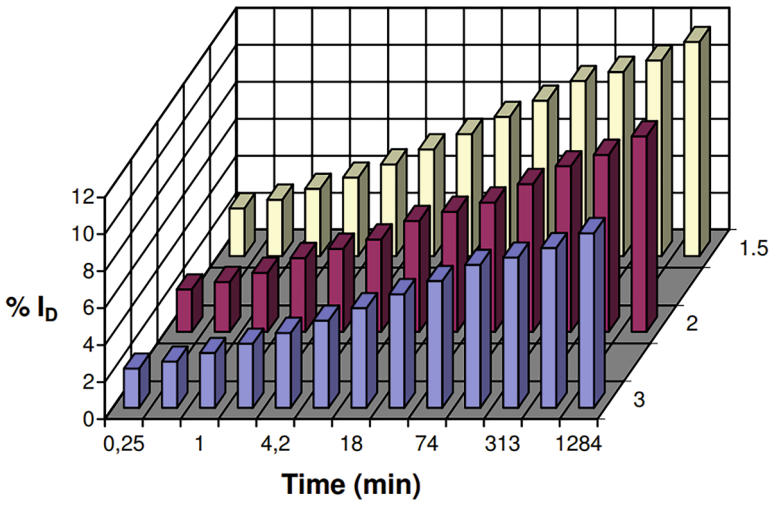

Fig. 2.3 Experimentally determined dependence of the drain current on channel length and stress time [21]

Table 2.2 Obtained functions of the investigated methods [21]

Investigation method	Obtained function
Power	$\%I_D(t,L) = k \cdot L^m \cdot t^n$
Logarithmic	$\%I_D(t,L) = k \cdot L^m + n \ln(t)$
Weibull	$\%I_D(t,L) = 1 - \exp(-(t/k \cdot L^m))^n$

Table 2.3 Obtained function coefficients of PMOS transistors for different methods [21]

	Power	Logarithmic	Weibull
$I_D(V_D = 0.5\,V)$	$k = 3.158$ $m = -1.175$ $n = 0.1216$	$k = 3.036$ $m = 1.199$ $n = 0.583$	$k = 270$ $m = 3.62$ $n = 0.174$
$I_D(V_D = 2.5\,V)$	$k = 1.372$ $m = -1.818$ $n = 0.156$	$k = 1.261$ $m = 1.115$ $n = 0.370$	$k = 40{,}052$ $m = 4.7$ $n = 0.181$
$I_D(V_G = 1.5\,V)$	$k = 3.264$ $m = -1.982$ $n = 0.156$	$k = 3.005$ $m = 1.982$ $n = 0.8833$	$k = 16{,}400$ $m = 2.95$ $n = 0.26$
$I_D(V_G = 2\,V)$	$k = 1.662$ $m = -1.677$ $n = 0.156$	$k = 1.531$ $m = 1.719$ $n = 0.4498$	$k = 13{,}160$ $m = 5.547$ $n = 0.36$
$I_D(V_G = 2.5\,V)$	$k = 1.513$ $m = -1.758$ $n = 0.156$	$k = 1.393$ $m = 1.741$ $n = 0.4094$	$k = 26{,}340$ $m = 3.44$ $n = 0.48$

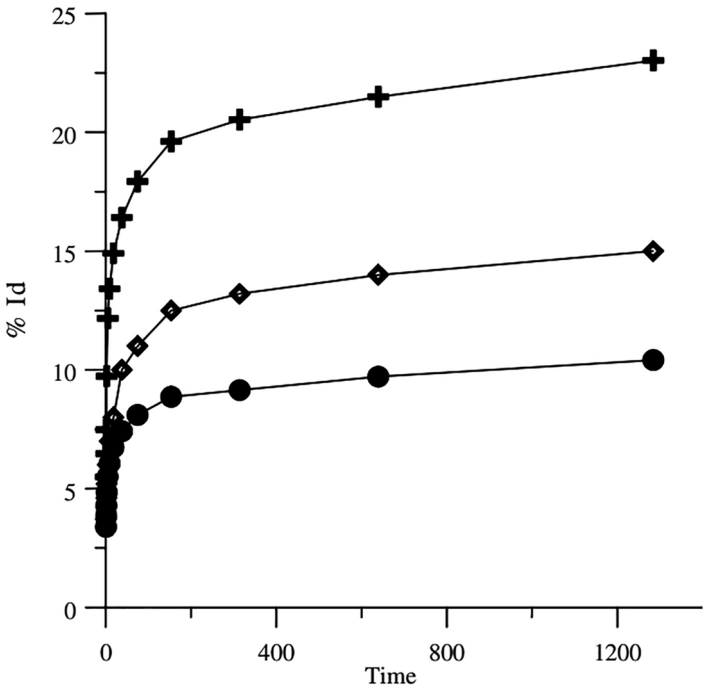

Fig. 2.4 Measured L = 1.5(+), 2 (◊), and 3(•) μm, and calculated (—) I_D % variations with the logarithmic method for different channel lengths (V_D = 0.5 V) [21]

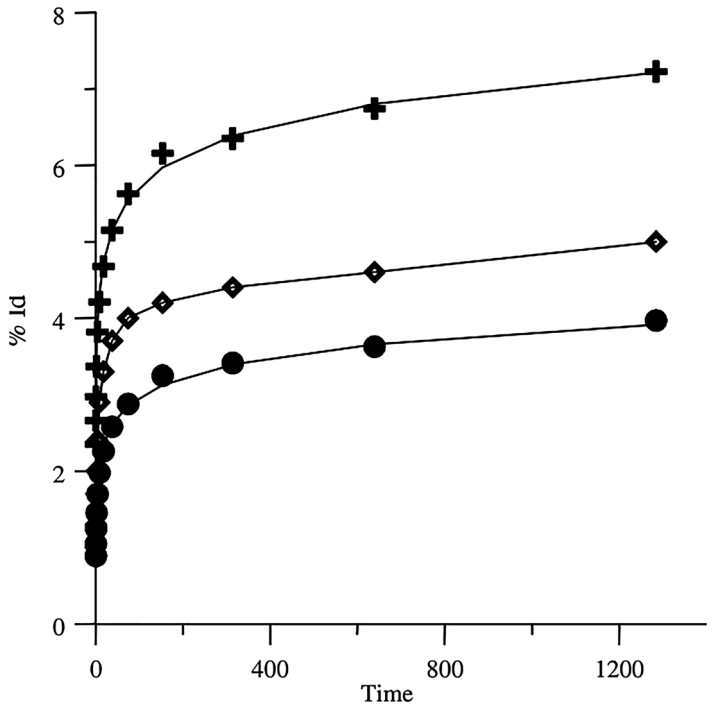

Fig. 2.5 Measured L = 1.5(+), 2 (◊), and 3(•) μm and calculated (—) I_D % variations with the logarithmic method for different channel lengths (V_D = 2.5 V) [21]

time-dependent functions, a solution was formed for the increasing value of the drain current by the connection of a dependent current source between the drain and source of the PMOS transistor, which was formed for increasing the value of the threshold voltage by the connection of a dependent voltage source to the gate. The proposed model for the PMOS can be seen in Fig. 2.7.

Concluding Remarks for PMOS Modeling

The effect of hot carriers on the drain current and threshold voltage of PMOS transistors was investigated statistically and an alternative method was proposed to those available in the literature. Three different statistical methods for PMOSs were investigated for modeling the hot-carrier degradation of transistors. In all the investigated methods, the change in hot carriers has been expressed by using two variable functions, and these coefficients can be determined independently of the technology of the transistor and its operating conditions. Considering the correlation coefficients of the investigated methods, we observe that the logarithmic method is the nearest method to 1 with 0.998, and, considering the RMS errors, we see that the

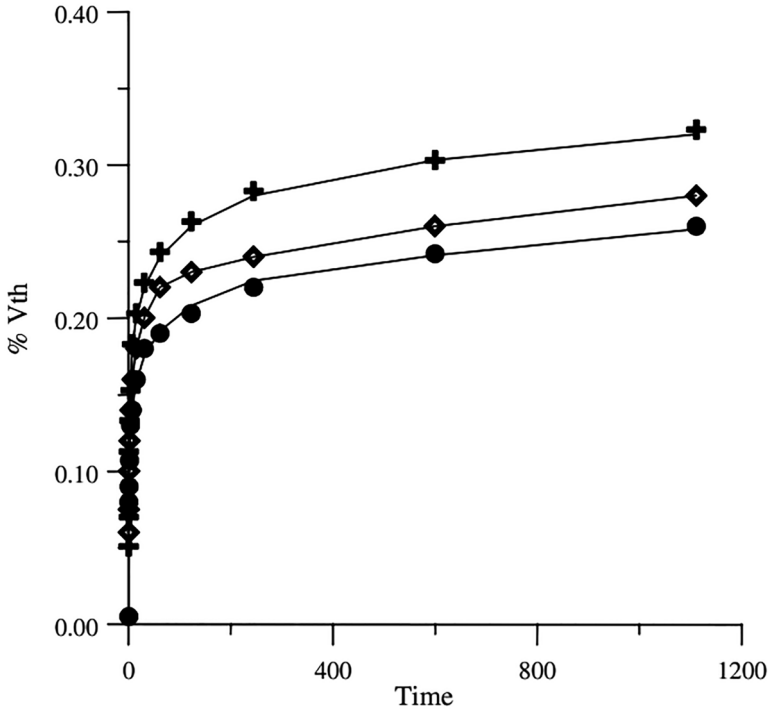

Fig. 2.6 Measured L = 1.5(+), 2 (◇), and 3(•) μm and calculated (—) V_{TH} % variations with the logarithmic method for different channel lengths (V_D = 2.5 V) [21]

Table 2.4 Obtained correlation coefficients for PMOS [21]

	Logarithmic	Power	Weibull
Id (Subthreshold)	0.998482	0.990399	0.997737
Id (Inversion)	0.997117	0.988502	0.992571
Vth	0.998128	0.952594	0.9587

logarithmic method has the least error with 0.03. From these results, we can say that the logarithmic method is the best method for the explanation of the change in the data. To express the variations in drain current and threshold voltage, models have been proposed for PMOS transistors by using the functions belonging to the investigated methods. By using these proposed methods, the effect of hot-carrier degradation on the CMOS inverter circuit was investigated. Hot-carrier degradation's effect on the performance of the circuit was discussed again by using SPICE simulations with the proposed models. At the end of this work, a lifetime prediction calculation was performed using the proposed functions. The proposed model has some advantages: it can be modeled more practically than the physical model and the simulation time is shorter than the physical model. The proposed method is based on the measurement results and it is independent of the technology; it can easily be

Table 2.5 Obtained RMS errors for PMOS [21]

	Logarithmic	Power	Weibull
Id (Subthreshold)	0.03111	0.07891	0.04657
Id (Inversion)	0.02728	0.04356	0.08093
Vth	0.01377	0.05528	0.08590

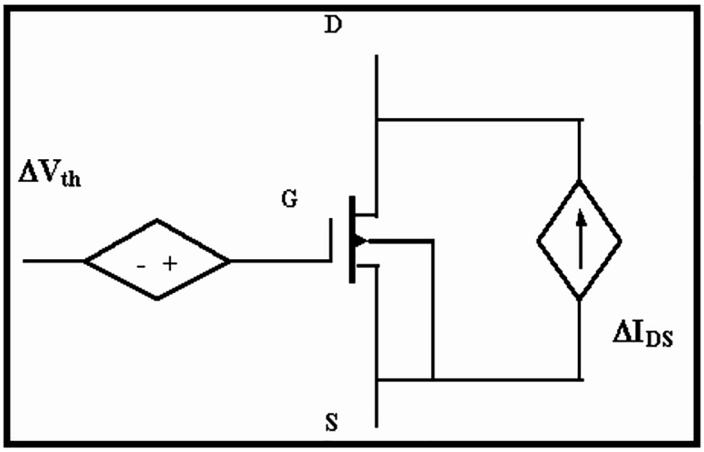

Fig. 2.7 Model to represent time-dependent variation of drain current and threshold voltage caused by the hot-carrier effect [21]

applied to PMOS transistors that have different dimensions. By using this proposed method, percentage changes in drain current, which occur as a result of degradation at any time (t) and threshold voltage, can be found and used for the lifetime prediction of the transistor, and/or any other circuit can be approximately predicted.

Statistical Model of Hot-Carrier Degradation and Lifetime Prediction for NMOS Transistors

Modeling of Hot Carriers

It's known that hot-carrier-induced degradation on MOS transistors causes a reliability problem. In this respect modeling of hot-carrier-induced degradation on one transistor is not sufficient. At the same time, the model has to include the degradation effects on whole circuit, when a known characteristic of the circuit reaches a critical value or how characteristic changes after a critical time. Hot carriers and their effects on the circuits are modeled by two distinct methods. These methods are, respectively,

- Direct parameter method.
- New model method.

In direct parameter method, hot carriers are modeled by using any existent MOSFET model. In this method, additions or modifications are made on MOSFET model equations for modeling the hot carriers [15, 16]. In new model method, an additional model is added to simulation program. Hot carriers are modeled by using this additional model [17, 18]. Both models have superiorities with respect to other model which are given as below

(a) Direct parameter method can be only used for selected MOSFET model but new model can be used for all simulation programs.
(b) Direct parameter method is established on an existing model, because of this fundamental reason improvement of it easy according to constitution of a new model.

Statistical Methods

This study was performed for five different transistors produced with the same technology but with different channel lengths. Process parameters of the used transistors are given as t_{ox} = 20 nm, x_j = 400 nm, the dimensions W = 10 µm, L = 1 µm, L = 1.2 µm, L = 1.5 µm, L = 2 µm, L = 3 µm. Stress voltage was applied to the transistors for a duration of 16 h. Statistical methods are applied and investigated by using variation of drain currents and threshold voltages with time which are obtained as a results of applied stress voltage (V_D = 0.1 V, V_D = 3 V, V_G = 1 V, V_G = 2 V, and V_G = 3 V). Calculations are based on linear regression method for the four approaches and least squares methods have been used [17, 18, 21]. So, calculations were performed by using MATLAB program in basis of Table 2.1.

1. Exponential Distribution with Least Squares Method:

$$y = Ae^{Bx} \tag{2.1a}$$

$$a = \frac{\sum_{i=1}^{n} \ln y_i \sum_{i=1}^{n} x_i^2 - \sum_{i=1}^{n} x_i \sum_{i=1}^{n} \left(x_i \ln y_i\right)}{n\sum_{i=1}^{n} x_i^2 - \left(\sum_{i=1}^{n} x_i\right)^2} \tag{2.1b}$$

$$b = \frac{n\sum_{i=1}^{n} x_i \ln y_i - \sum_{i=1}^{n} x_i \sum_{i=1}^{n} \ln y_i}{n\sum_{i=1}^{n} x_i^2 - \left(\sum_{i=1}^{n} x_i\right)^2} \tag{2.1c}$$

where $B \equiv b$ and $A \equiv \exp(a)$.

2. Logarithmic Distribution with Least Square Method:

$$y = a + b\ln(x) \tag{2.2a}$$

$$a = \frac{\sum_{i=1}^{n} y_i - b\sum_{i=1}^{n} \ln x_i}{n} \tag{2.2b}$$

$$b = \frac{n\sum_{i=1}^{n}(y_i \ln x_i) - \sum_{i=1}^{n} y_i \sum_{i=1}^{n} \ln x_i}{n\sum_{i=1}^{n}(\ln x_i)^2 - \left(\sum_{i=1}^{n} \ln x_i\right)^2} \tag{2.2c}$$

3. Power Distribution with Least Square Method:

$$y = A\mathrm{e}^{Bx} \tag{2.3a}$$

$$a = \frac{\sum_{i=1}^{n} y_i - b\sum_{i=1}^{n} \ln x_i}{n} \tag{2.3b}$$

$$b = \frac{n\sum_{i=1}^{n}(\ln y_i \ln x_i) - \sum_{i=1}^{n} \ln x_i \sum_{i=1}^{n} \ln y_i}{n\sum_{i=1}^{n}(\ln x_i)^2 - \left(\sum_{i=1}^{n} \ln x_i\right)^2} \tag{2.3c}$$

where $B \equiv b$ and $A \equiv \exp(a)$.

Numerical Results

It can be seen from experimental results that the drain current and the threshold voltage of NMOS transistors decreases with time. On the other hand, from a previous study [10], it can be easily observed that the drain current and the threshold voltage of PMOS transistors increases with time. For L = 1.5 μm, the change in the drain current is approximately 4% for PMOS, while it is 0.8% for NMOS. The functions, obtained by using investigated methods, that give the percent changes in drain currents and threshold voltages are given in Table 2.6. The function coefficients obtained of four methods for different channel lengths can be seen in Table 2.7.

Calculated results are compared with experimental results. It has been observed that the Power-log-II method seems to be the best statistical method that characterizes the measurement results. The characterization results, using Power-Log-II method, are given with experimental results (absolute values) in Figs. 2.8 and 2.9. It seems from the figures that there is a good agreement between the experimental

Table 2.6 Obtained functions of investigated methods [25]

Investigation method	Obtained function
Power	$\%I_D(t,L) = k \cdot L^m \cdot t^n$
Power-Log-I	$\%I_D(t,L) = k \cdot L^m \cdot n \ln(t)$
Power-Log-II	$\%I_D(t,L) = k \cdot L^m \cdot t^n \cdot \ln(t)$
Weibull	$\%I_D(t,L) = 1 - \exp(-(t/k \cdot L^m))^n$

Table 2.7 Obtained function coefficients of NMOS transistors for different methods [25]

	Power	Power-Log-I	Power-Log-II	Weibull
$I_D(V_D = 0.1\,V)$	$k = 1.076$ $m = -1.175$ $n = 0.3267$	$k = 0.345$ $m = -1.181$ $n = 1.757$	$k = 0.562$ $m = -1.19$ $n = 0.141$	$k = 0.87 \times 10^6$ $m = 3.62$ $n = 0.345$
$I_D(V_D = 3\,V)$	$k = 0.01908$ $m = -1.818$ $n = 0.572$	$k = 0.0008$ $m = -1.795$ $n = 3.66$	$k = 0.008$ $m = -1.815$ $n = 0.413$	$k = 0.14 \times 10^3$ $m = 4.7$ $n = 0.83$
$I_D(V_G = 1\,V)$	$k = 0.06235$ $m = -1.982$ $n = 0.36$	$k = 0.0112$ $m = -1.841$ $n = 2.158$	$k = 0.027$ $m = -1.845$ $n = 0.191$	$k = 0.18 \times 10^4$ $m = 2.95$ $n = 0.46$
$I_D(V_G = 2\,V)$	$k = 0.0286$ $m = -1.677$ $n = 0.486$	$k = 0.0028$ $m = -1.7$ $n = 2948$	$k = 0.014$ $m = -1.719$ $n = 0.311$	$k = 0.12 \times 10^3$ $m = 5.547$ $n = 0.66$
$I_D(V_G = 3\,V)$	$k = 0.0229$ $m = -1.758$ $n = 0.545$	$k = 0.0012$ $m = -1.733$ $n = 3.46$	$k = 0.0099$ $m = -1.741$ $n = 0.384$	$k = 0.34 \times 10^3$ $m = 3.44$ $n = 0.8$

results and calculated values. To show the similarity between the measured and calculated values, correlation coefficients were calculated and very highly correlated coefficients were obtained. Results obtained can be seen in Table 2.8. Moreover, error calculations are achieved with RMS method and the results are given in Table 2.9. It can be easily observed that the error values are very low. With respect to graphics, correlation coefficients and RMS errors, the methods are classified from the best to worst as Power-Log-II, Power-Log-I, Power and Weibull methods, respectively.

Experimental results at different stress conditions for NMOS transistors are summarized in the three-dimensional plots of $I_D = I_D(L,t)$ illustrated in Fig. 2.10. As it can be observed from Fig. 2.10 that the drain current decreases with the stress time; furthermore, I_D also decreases with the channel length.

It is apparent from experimental results on test transistors that the drain current and the threshold voltage of NMOS transistors decreases with time. On the other hand, experimental results also show that the drain current and the threshold voltage of PMOS transistors increases with time. The changes in the threshold voltage and in the drain current are represented by connecting a time-dependent voltage source series to the gate and a time-dependent current source parallel to drain-source terminals. According to the observed device behavior, these sources are filled with adequate statistical expressions. The related reliability model for NMOS transistors is illustrated in Fig. 2.11.

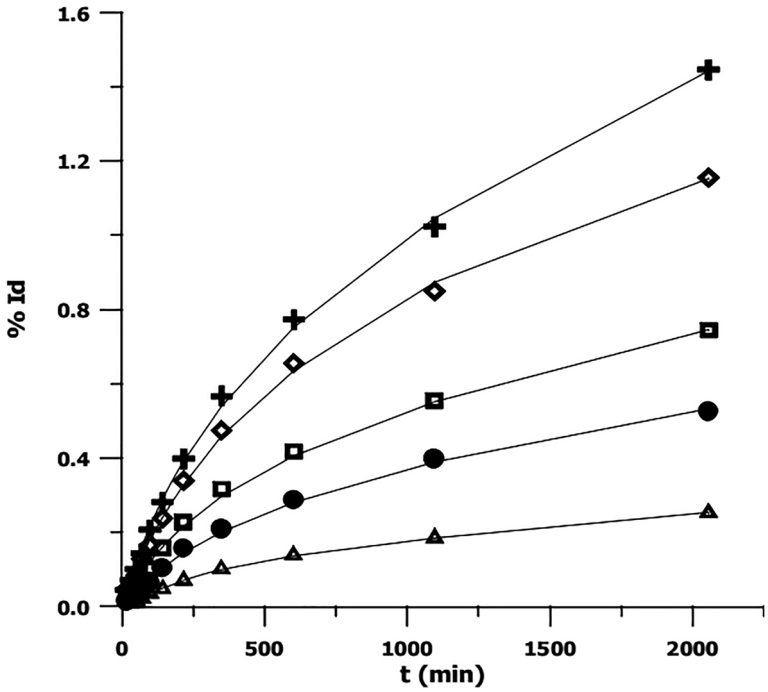

Fig. 2.8 Measured L = 1(+),1.2 (◇), 1.5 (□), 2(●), 3(Δ)μm and calculated (—) % I_d variations with Power-Log-II method for different channel lengths [25]

Lifetime Prediction

Lifetime prediction for NMOS transistors has been performed by using the criteria given in literature [18–25]. It can be reached easily to a 10% lifetime criteria of hot carriers in DC stress application without more time than 10 years. One year in static conditions show 10 years in real operating condition point in analog application. Life time prediction calculations for NMOS were performed with respect to Power-Log-II method by using the functions at the proposed methods and 10% drain current criteria which is given in the literature [18]. Lifetime prediction results obtained by calculations for different channel lengths and different operating regions can be seen in Table 2.10.

Concluding Remarks for NMOS

In this study, the effect of hot carriers on the drain current and threshold voltage of NMOS transistors were investigated statistically and a method was proposed to be an alternative to those available in the literature. At the end of the investigation, it

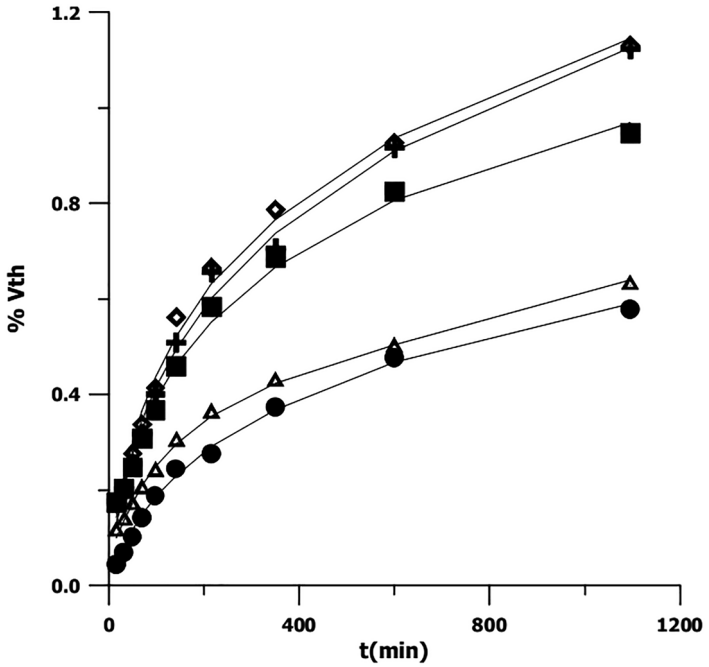

Fig. 2.9 Measured L = 1(+),1.2 (◊), 1.5 (□), 2(●), 3(Δ)μm and calculated (—) % V_{TH} variations with Power-Log-II method for different channel lengths [25]

Table 2.8 Obtained correlation coefficient for NMOS [25]

Channel length (μm)	Power	Power-Log-I	Power-Log-II	Weibull
L = 1	0.99614	0.99587	0.99732	0.99615
L = 1.2	0.99540	0.99613	0.99710	0.99536
L = 1.5	0.99705	0.99527	0.99744	0.99710
L = 2	0.99782	0.99593	0.99818	0.99777
L = 3	0.99743	0.99840	0.99927	0.99704

Table 2.9 Obtained RMS error NMOS [25]

Channel length (μm)	Power	Power-Log-I	Power-Log-II	Weibull
L = 1	0.00702	0.00736	0.00582	0.00731
L = 1.2	0.00672	0.00622	0.00529	0.00689
L = 1.5	0.00404	0.00522	0.00377	0.00401
L = 2	0.00269	0.00376	0.00248	0.00277
L = 3	0.00147	0.00117	0.00077	0.00168

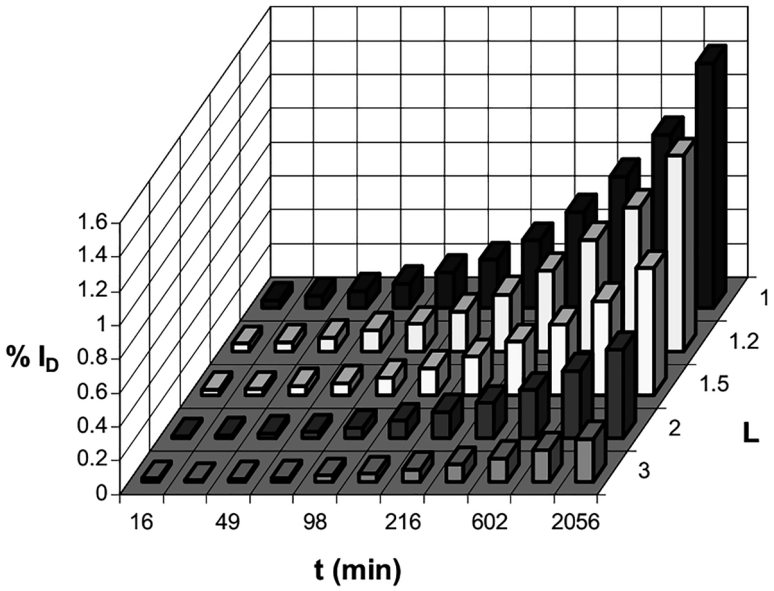

Fig. 2.10 Experimentally determined dependence of the drain current, on the channel length and on the stress time [25]

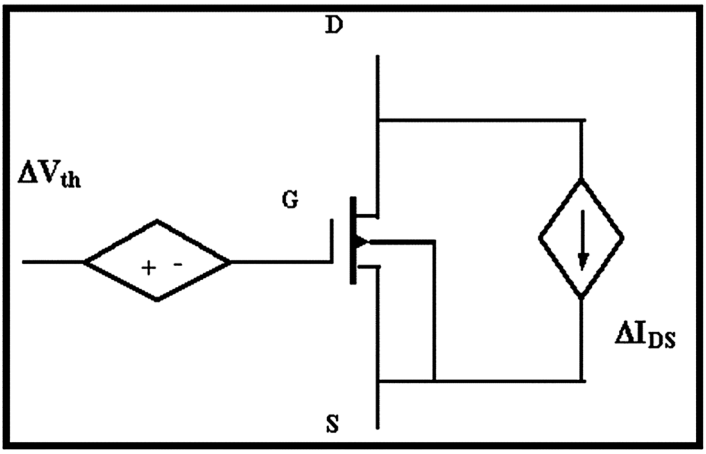

Fig. 2.11 The related reliability model for NMOS transistors [25]

was seen that the drain current and the threshold voltage decreased with time for NMOS transistors. Power, Power-Log-I, Power-Log-II, and Weibull statistical methods were investigated by using variation of drain current and threshold voltage with time which is obtained for applied stress voltage. Coefficients are optimized with these methods and functions are generated. These functions give variation of

Table 2.10 NMOS calculated prediction lifetime for different channel length [25]

	NMOS predicted lifetime (s)	
Channel length (μm)	Subthreshold region	Inversion region
$L = 1$	9.3×10^2	3.7×10^5
$L = 1.2$	1.8×10^3	1.0×10^6
$L = 1.5$	9.1×10^3	1.8×10^7
$L = 2$	5.1×10^4	5.8×10^7
$L = 3$	3.1×10^6	6.8×10^9

drain current with time and channel length. The suggested method can be suitable for PMOS and NMOS transistors with different dimensions because it depends on the measured values. Once observed and specified for transistors manufactured with a MOS process the observation results can be applied to the SPICE NMOS and PMOS device models. By using this proposed method, percentage changes in drain current which occur as a result of degradation at any time t, and threshold voltage can be find and used for the lifetime prediction of the transistor.

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Chapter 3
Demonstration of Proposed Method with Application Examples

The advantages provided by the method proposed is demonstrated on application examples [1–3], namely on the properties of a current source-loaded single-stage amplifier, on a CMOS inverter and on a CMOS OTA, operating in subthreshold region. Note that the CMOS OTA operating in subthreshold region is also described in the related next chapter.

Basic Concept

The reliability of a system is defined as the probability that it will perform its required function under stated conditions for a stated period of time. Rapid changes in the technology, shorter periods in product development, and higher reliabilities of products make accelerated life tests even more useful and important in the industry of today [1–58]. Accelerated life tests are used to obtain timely information on the times to failure distributions of components and systems [4–7]. Test units are subjected to higher than the usual levels of stress. Then the test results are extrapolated from the test conditions to the usual use conditions via physically reasonable statistical models. Models based on Weibull statistics are widely used as accelerated-life-test models in reliability engineering [4–8]. Several works on Weibull statistical models and their applications were performed and results obtained in the frame of these works were published in the literature [9–11]. Because of the increasing densities of VLSI chips, the importance of long-term reliability in MOS VLSI circuits is also becoming an important issue. The reliability on the circuit level is directly related to the observed physical failure mechanisms. Some of physical degradation mechanisms such as electromigration and electrostatic discharge manifest themselves by abrupt and catastrophic changes in the device characteristics and the circuit operation. Other mechanisms such as hot-carrier effects cause noncatastrophic failures which develop gradually over time and change the circuit performance. For

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most failure mechanisms concerning MOS VLSI circuits, the system cannot be repaired and returned to normal use once a failure occurs [12–20]. Hot-carrier-induced phenomena influences transistor performance parameters such as threshold voltage and drive currents in all operating regimes; it therefore continues to create great interest because of its important role in device reliability. Several works were performed for investigation of hot-carrier effect on the performance of NMOS and PMOS transistors and for digital and analog cases [14–33]. It has been recognized that the degradation of NMOS transistors is caused by the interface state generation and electron trapping in the gate oxide from the hot-carrier injection. Reliability assurance of analog circuits requires a largely different approach than for the digital case. The hot-carrier degradation of PMOS is investigated from the viewpoint of analog operation [20, 21, 27]. In a recent work, a method is presented that allows to quantify the effects of hot-carrier degradation on analog CMOS circuits. Specific features of hot-carrier degradation related to analog CMOS operation are discussed in detail [20].

One of the most important goals of hot-carrier considerations related to analog operation is to enable the prediction of circuit parameter degradation on the basis of simple, standard single transistor stress experiments. Note that the methods presented for modeling the hot-carrier degradation are based almost on experimental observations. The main difficulty in modeling the influence of the hot carriers on MOS transistor behavior is the determination of the values for physical quantities [20, 22]. Investigation of the recent works proves the necessity of a simple approach for representation of hot-carrier effect on the MOS transistor threshold voltage.

The aim of this section is to propose a new representation of the hot-carrier degradation in threshold voltage of MOS transistors by applying the Weibull distribution to the experimental observations and to predict the device behavior after a long stress time. Firstly, a brief information on the hot-carrier effect is given. In the next section, Weibull distribution is considered in detail. Further part delivers experimental results and an application example. Theoretical results are compared with experimental results. The advantage of the proposed approximation is proven on an analog test circuit.

Hot Carrier Effects

By the advances in VLSI fabrication technologies, the reduction of device dimensions such as the channel length, the junction depth, and the gate oxide thickness without proportional scaling of the power supply voltage, results in significant increase of the horizontal and vertical electric field in the channel region. Hot-carrier-induced degradation of MOS transistors is caused by the injection of high-energy electrons and holes into the gate oxide [13–15]. The oxide damage is in the form of charge trapping and/or interface trap generation which gradually builds up changes the current–voltage characteristics of the transistor. Hot-carrier effects

cause gradual changes in device characteristics during circuit operation. Although the circuit performance is ultimately affected by these changes, the continuous nature of degradation mechanisms presents some special challenges in analysis and estimation of reliability. The damage caused by hot-carrier injection affects the transistor characteristics by causing a degradation in transconductance, a shift in the threshold voltage and a change in the drain current capability. This degradation in the device leads to the degradation of circuit performance over time.

Weibull Distribution

The Weibull distribution is often used to describe the life times of parts [7]. When a number of parts are put on a test, they do not all fail at the same time. If parts fail according to a Weibull distribution, the probability that any single part will fail at a particular time as follows:

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\alpha}\right)^{\beta}\right] \tag{3.1}$$

where "a" is called the scale parameter, "b" is called the shape parameter, and F is called the cumulative distribution function. The values of a and b are estimated from the data by using linear regression (1) maximum likelihood or graphical plotting technique [7]. Substituting a and b into the formula we can calculate F (the probability of failure) at any time, t. The reliability function is calculated by the formula:

$$R(t) = 1 - F(t) = \exp\left[-\left(\frac{t}{\alpha}\right)^{\beta}\right] \tag{3.2}$$

When we perform a regression fit of a straight line to a set of (x, y) data points we typically minimize the sum of squares of the "vertical" distance between the data points and the line. The correlation coefficient shows the statistical dependence of a non-functional relation between two variables. The value of the correlation coefficient (ρ) changes between -1 and $+1$ extremums ($-1 < \rho < +1$). If the correlation coefficient ρ has a value near ± 1, it defines a strong and linear relation. If $\rho = 0$, it means that the variables are statistically independent. Suppose that we observe an event with two variables. If we change the values of one variable which can be controlled, the any other variable will have an interval of "possible values". The variable which can be controlled is called the independent variable and the other one which cannot be controlled is called the dependent variable. In this study, we accept time as independent variable and the measured current and voltage percentage changes as dependent variable.

Experiments and Application Example

Experiments were performed on NMOS test transistors fabricated in TUBITAK MAM-YITAL (Marmara Research Center YITAL Laboratory, The Scientific and Technical Research Council of Turkey) with 3-μm technology [1]. The dimensions of these NMOS transistors were $W = 27$ μm, $L = 3$ μm. The test circuit to apply a stress on the MOS transistors is illustrated in Fig. 3.1. The experiments were realized with semiconductor parameter analyzer HP 4155 at Istanbul Technical University (ITU) Electronics Laboratory. Applying a stress voltage of $V_D = 5$ V and choosing the gate biasing voltage as $V_G = 1$ V, $V_G = 1.5$ V, and $V_G = 2$ V, respectively, to provide different stress conditions, the transfer characteristic of the test device was observed and recorded for a time period of 10 h with a time step of 30 min; the experimental data obtained is used to determine the threshold voltage V_{th}. The same process is repeated on several samples of NMOS transistors with the same properties. To demonstrate that the method proposed is independent of the manufacturing technology, similar experiments were also performed for CD4007 NMOS array transistors ($W = 305$ μm, $L = 14$ μm) which is the yield of a fully different technology. The stress conditions for experiments are given in Table 3.1. Experimental results at different stress conditions for TUBITAK NMOS transistors ($W = 27$ μm, $L = 3$ μm) and for CD4007 NMOS transistors ($W = 305$ μm, $L = 14$ μm) are summarized in the three dimensional plots of $V_{th} = V_{th}(V_G, t)$ illustrated in Fig. 3.2a, b. As it can be observed from Fig. 3.2, the threshold voltage decreases with the stress time; furthermore, V_{th} also decreases with the gate stress voltage V_G.

Experimental results at different stress conditions for TUBITAK NMOS transistors ($W = 27$ μm, $L = 3$ μm) and for CD4007 NMOS transistors ($W = 305$ μm, $L = 14$ μm) are summarized in the three dimensional plots in Fig. 3.2a, b. As it can be observed from Fig. 3.2, the threshold voltage decreases with the stress time; furthermore, V_{th} also decreases with the gate stress voltage V_G.

By using experimental data and the linear regression method, the Weibull parameters are calculated and results obtained are illustrated in Table 3.2. The changes in the threshold voltage V_{th} are estimated for NMOS transistors by the use of Weibull parameters in Table 3.2 and Eq. (3.1). The estimated and the measured V_{th}% against

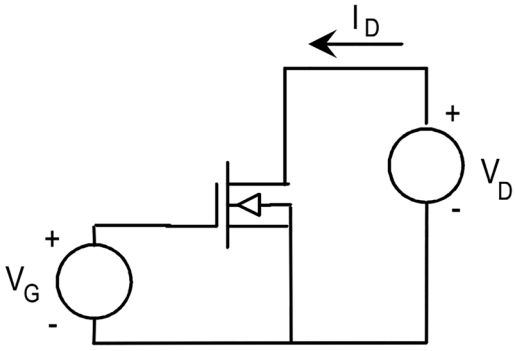
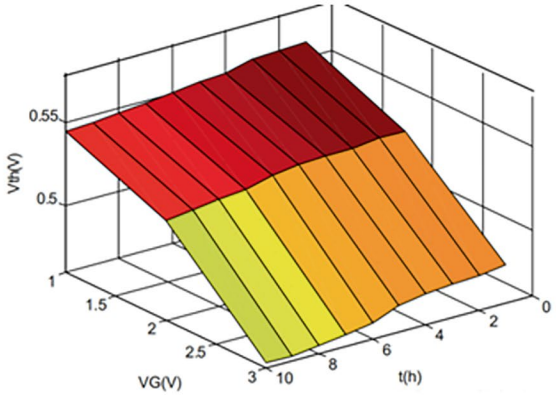


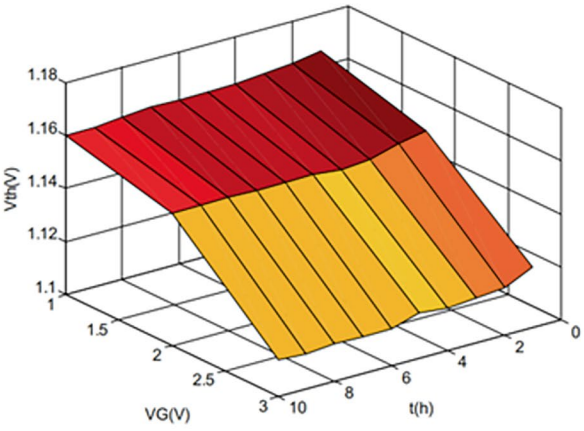
Fig. 3.1 Test circuit to apply a stress on the MOS transistor realized with semiconductor parameter analyzer HP4155 [1]

Table 3.1 Stress conditions for two different NMOS transistors experiments [1]

Stress conditions	
TUBITAK 3-μm NMOS transistor	CD 4007 NMOS array transistors
$V_D = 5$ V, $V_G = 1$ V	$V_D = 10$ V, $V_G = 1$ V
$V_D = 5$ V, $V_G = 1.5$ V	$V_D = 10$ V, $V_G = 3$ V
$V_D = 5$ V, $V_G = 2$ V	$V_D = 10$ V, $V_G = 5$ V



a)



b)

Fig. 3.2 Experimentally determined dependence of the threshold voltage (V_{th}) on the gate voltage (V_G) and on the stress time (t) obtained for: (**a**) NMOS transistors produced by TUBITAK with 3-μm technology ($W = 27$ μm, $L = 3$ μm) and (**b**) CD4007 type array transistor [1]

Table 3.2 The Weibull parameters which are used to calculate the estimated values of V_{th} variations, the correlation coefficients, and of TUBITAK 3-μm NMOS transistors and CD4007 array transistors [1]

Stress conditions	Shape parameter, β	Scale parameter, α	Correlation coefficient
TUBITAK 3 μm NMOS transistor			
V_D = 5 V, V_G = 1 V	1.0727	1.48E + 02	0.811241
V_D = 5 V, V_G = 1.5 V	1.45316	8.92E + 01	0.978418
V_D = 5 V, V_G = 2 V	1.2567	8.21E + 01	0.969851
CD 4007 NMOS array transistors			
V_D = 10 V, V_G = 1 V	0.73003	1.84E + 04	0.956304
V_D = 10 V, V_G = 3 V	0.962096	1.97E + 03	0.956901
V_D = 10 V, V_G = 5 V	1.01323	1.37E + 03	0.945853

stress time plots of TUBITAK 3 μ NMOS transistors for a stress condition of V_D = 5 V, V_G = 2 V are shown in Fig. 3.3a. Figure 3.3b illustrates estimated and measured plots of V_{th}% against stress time related to CD4007 type array transistor for a stress condition of V_D = 10 V, V_G = 3 V. It can be easily seen from figures that the estimated and the measured values are in good agreement. Similar characteristics are observed for the other stress conditions given in Table 3.1.

The reliability curves of V_{th} at three different operating points are obtained for both transistors and are shown in Fig. 3.4. Note that the reliability curve can be considered as a measure of the influence of possible degradations in device parameters on device reliability during the operation time, if the measurement conditions are still valid for further operations. Therefore, the device reliability can be provided only, if the device parameter variations remain in specified limits. It should be mentioned that the reliability curves for the decrease in the threshold voltage are to be drawn for these specified limits to get meaningful results. Note that the hot-carrier failure can initiate the electron/hole trapping/generation and/or interface trap creation mechanism leading to changes of oxide charge and trap densities during device operation. For a complete physical representation, the influence of hot carriers on the space charge, on the surface potential, and on the flatband voltage must be taken into consideration [1]. After hot-carrier degradation, the space charge region at the drain end increases or decreases depending on the type of hot-carrier degradation effect. The hot-carrier degradation affects the space charge region in all operation mode of the MOSFET. Similarly, the discontinuities at the crystal surface, dangling bonds, and miscellaneous impurities increase after hot-carrier degradation which increases or decreases the surface potential depending on the type of hot-carrier degradation effect. As a result, the threshold voltage may increase or decrease with the stress time. Note that the Weibull distribution method is capable to estimate the change in the threshold voltage for both cases if sufficient data is available. The advantages provided by the method proposed is demonstrated on an application example, namely on the properties of the current source-loaded single-stage

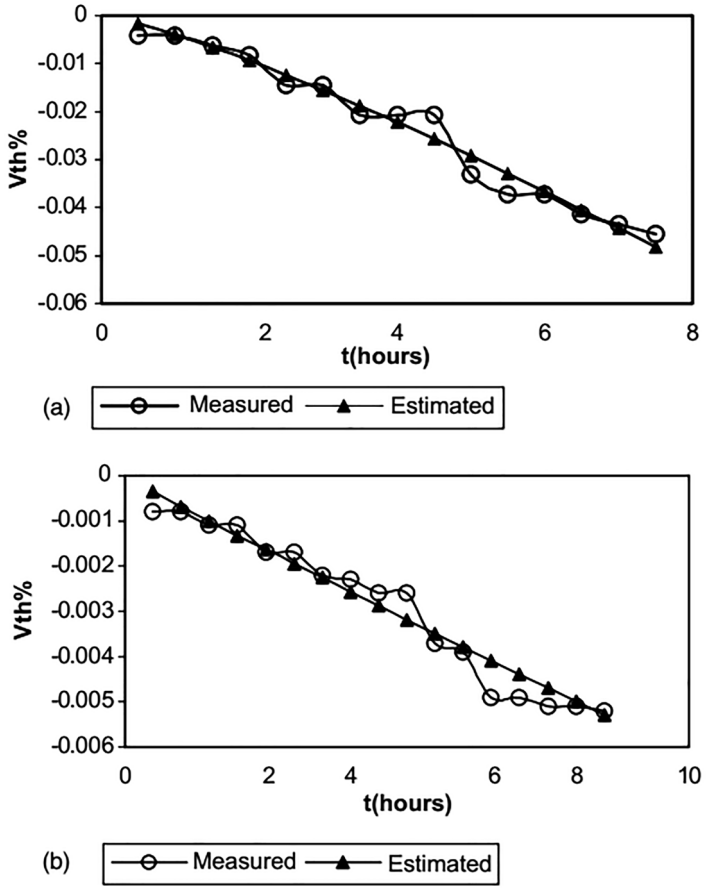


Fig. 3.3 Measured and with Weibull distribution estimated plots of V_{th}% against stress time: (**a**) NMOS transistors produced by TUBITAK with 3 μ technology for $V_D = 5$ V, $V_G = 2$ V stress condition and (**b**) CD4007 type array transistor for $V_D = 10$ V, $V_G = 3$ V [1]

amplifier shown in Fig. 3.5, which is mostly used as an intermediate stage in operational amplifiers, OTAs, and audio amplifiers. Furthermore, it was shown in recent works that the total harmonic distortion of the active-loaded single stage amplifier depends strongly on the operating point where the total harmonic distortion crosses through a minimum at a special biasing point [33–36].

Any shift in operating point influences, the harmonic distortion properties of the amplifier, which is demonstrated by SPICE simulations using a physical MOSFET model with extended accuracy intended especially for accurate simulation of analog building blocks where an improved representation of the channel length modulation is necessary [35, 36]. The supply voltage was $V_{DD} = 5$ V and the biasing current was chosen as $I_O = 200$ μA. A sinusoidal voltage of 1 kHz was applied to the input. Changing the input biasing voltage V_{IQ}, the operating point V_{OQ} is shifted along the

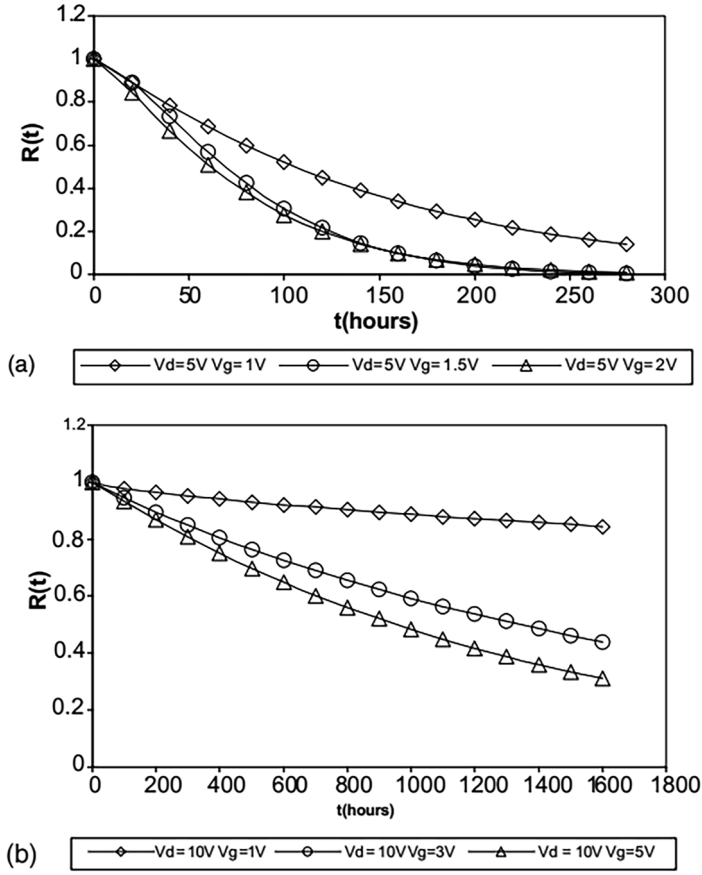


Fig. 3.4 The V_{th} variation reliability curves obtained from Weibull distribution of: (**a**) TUBITAK 3 μ NMOS transistor and (**b**) CD 4007 array transistor at three different operating points [1]

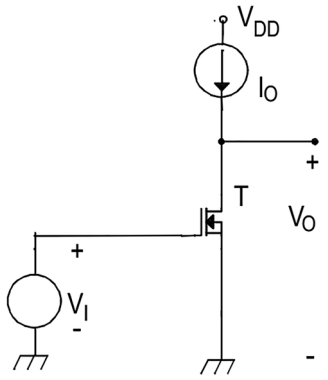


Fig. 3.5 Single-stage active-loaded MOS amplifier [1]

DC curve. The output signal amplitude was kept constant at V_{OP} = 100 mV at each operating point. Simulation results obtained for the case of non-stressed operation yield the plot of THD against the operating drain-source voltage V_{OQ} of the NMOS driver transistor illustrated in Fig. 3.6. Simulation results obtained with accurate model show that the total harmonic distortion crosses through a minimum point of $THD_{min} = 0.177\%$ at $V_{OQ} = 2.85$ V where the input biasing voltage is $V_{IQ} = 1.43$ V. The aim is to predict the changes in DC transfer curve and in the total harmonic distortion properties of the amplifier caused by hot-carrier degradation in the threshold voltage. For experiments, the load transistors were chosen as bipolar transistors to avoid any additional hot-carrier effect caused by PMOS load transistors. Measurements were performed by using HP 4155 Parameter Analyzer. The operating point of the amplifier was chosen at $V_O = 2.85$ V and $I_O = 200$ µA. The threshold voltage before the stress is specified as $V_{th} = 0.53$ V. The value of V_{th} decreases to $V_{th} = 0.5$ V after a stress of 10 h which can be also predicted by using the proposed method. The dependence of DC transfer curve on stress time is obtained experimentally and shown in Fig. 3.7.

Note that the operating point of the amplifier will be shifted on the DC transfer curve because of the hot-carrier degradation which causes a change in the minimum point of the total harmonic distortion. The mid-point of the transfer characteristic is specified as $V_{IM} = 1.44$ V and $V_{OM} = 2.5$ V. SPICE simulations result in a mid-point of $V_{IM} = 1.44$ V, $V_{OM} = 2.51$ V. After applying a stress of 10 h, the experimentally determined V_{OM} is shifted to $V_{OM} = 2.15$ V for $V_{IM} = 1.44$ V. With the predicted threshold voltage of 0.493 V, SPICE simulations result in $V_{OM} = 2.01$ V for

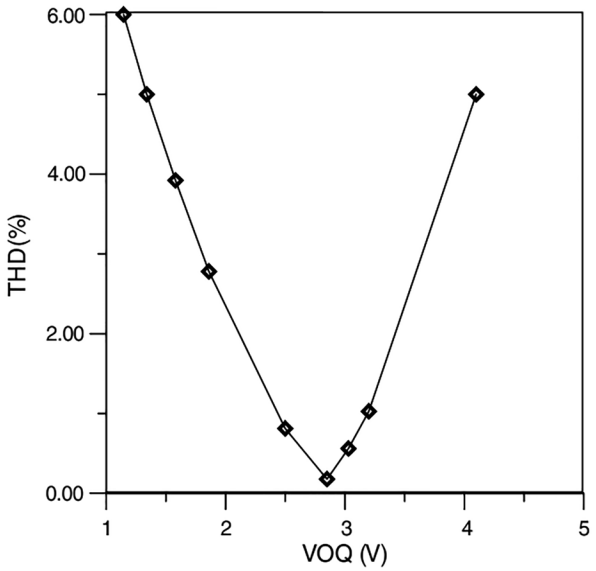


Fig. 3.6 Dependence of total harmonic distortion of active-loaded amplifier stage on operating point [1]

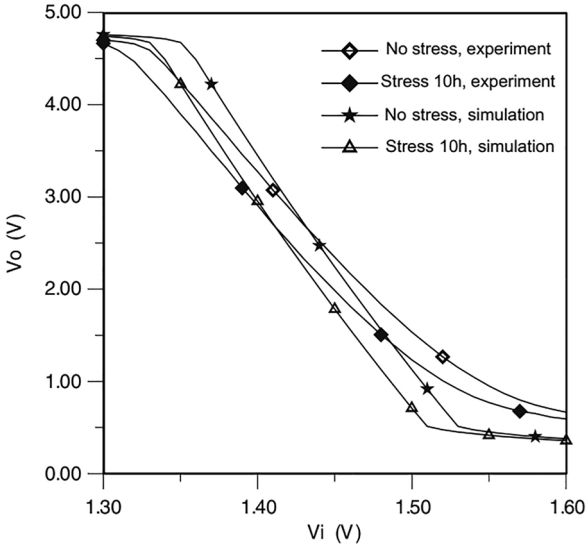


Fig. 3.7 Experimental and simulated dependence of DC transfer curve on stress time [1]

Table 3.3 The SPICE simulation results for the dependence of V_{th}, operating point and THD on stress time [1]

Stress time (h)	V_{th} (V)	V_I for V_O = 2.5 V	THD for V_I = 1.43 V (%)
0	0.53	1.44	0.177
5	051449	1.425	1.318
10	0.49368	1.405	3.495
15	0.47094	1.38	6.01
20	0.44733	1.36	8.48

V_{IM} = 1.44 V. Using the method proposed, the change in the MOS threshold voltage is calculated for stress times of 5, 10, 15, and 20 h, respectively. For each of these predicted values, the shift in the operating point of the amplifier and the total harmonic distortion THD for constant input biasing of V_{IQ} = 1.43 V are obtained by SPICE simulations and given in Table 3.3. From Table 3.3, it can be easily observed that the input biasing voltage providing a mid-point output voltage of V_{OQ} = 2.5 V decreases from V_{IQ} = 1.44 V to V_{IQ} = 1.36 V after a stress time of 20 h. This phenomenon is caused by the reduction in MOS threshold voltage due to hot-carrier degradation. For a constant input biasing voltage providing minimum total harmonic distortion, the operating point is shifted then from V_{OQ} = 2.85 V to V_{OQ} = 0.9 V after the same stress time, therefore an increase in the total harmonic distortion is observed at the output from its minimum value 0.177% to a much higher value of THD = 8.48%. It can be clearly seen from the results that the method proposed is useful to predict accurately the shift in the operating point caused by the change in the threshold voltage due to the hot-carrier effect. Note that experimental results are obtained for a maximum stress time of 10 h. Theoretical results are found to be in good agreement with experiments for this period. Starting from this good agreement

and using the Weibull distribution, the circuit behavior for longer stress times of 15 and 20 h can be also predicted, which demonstrates the prime importance of this work.

Concluding Remarks

In this study, the variations in the threshold voltage caused by the influence of hot-carrier effects are examined. A Weibull distribution-based new approach is proposed to represent hot-carrier degradation in the threshold voltage of MOS transistors. The estimated values calculated by the Weibull distribution are compared with the measured values. High correlation coefficients and accommodated results are obtained in most of the samples. The suggested method can be suitable for PMOS and NMOS transistors with different dimensions because it depends on the measured values. Once observed and specified for transistors manufactured with an MOS process, the observation results can be applied to the SPICE NMOS and PMOS device models. As a result, the prediction method proposed in the frame of this work will be helpful to estimate the influence of hot-carrier degradation to any circuits topology realized with the same MOS process. By the results of an SPICE simulation using this knowledge, it is possible to determine the influence of hot-carrier effects to the circuit performance in the course of time. This will especially supply facility in working for the analog integrated circuit designers.

Demonstration on an Application Example of CMOS Inverter

In this section, SPICE simulation of a CMOS inverter was performed to demonstrate how the proposed method can be applied to a circuit example and to show the practicality of the method. BSIM3 MOSFET model parameters, which are often used in simulations nowadays, were used. By using the simple CMOS structure shown in Fig. 3.8, circuit simulations were performed. Supply voltage of the circuit

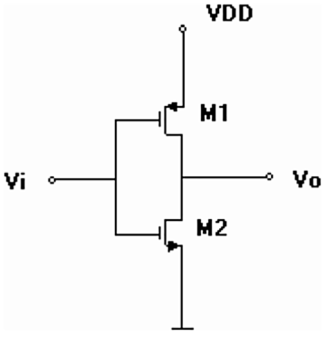


Fig. 3.8 CMOS inverter circuit [1]

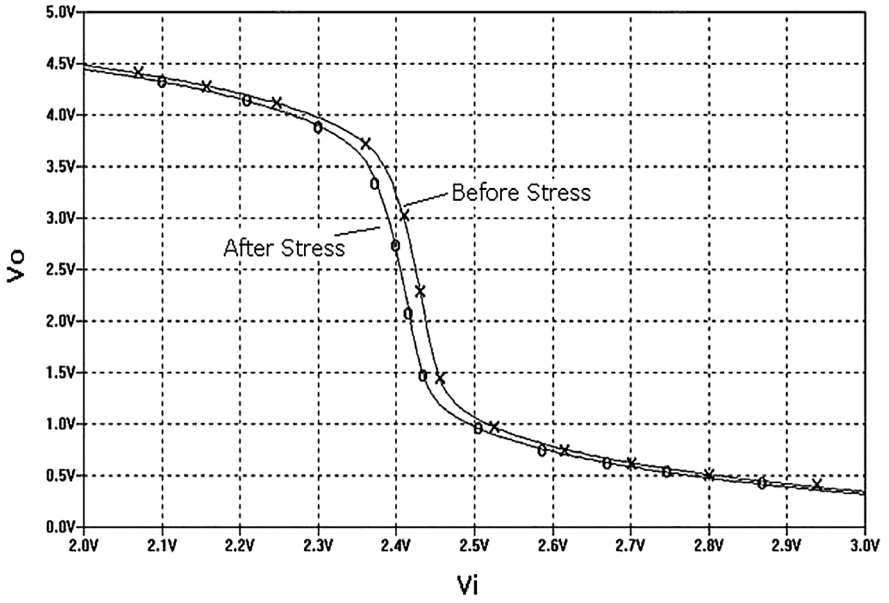


Fig. 3.9 Voltage transfer characteristics before and after stress of the CMOS inverter [1, 2]

was chosen as $V_{DD} = 5$ V, dimensions for the NMOS were $W = 10$ μ and $L = 3$ μ, and dimensions for PMOS transistors are $W = 10$ μ and $L = 1.5$ μ.

SPICE simulation results for the change in the DC transistor characteristics of the circuit, before stress and after stress, are shown in Fig. 3.9. In CMOS inverters, the change of the current and threshold voltage of the transistors has an important effect on the value of the inverting voltage of the circuit. Inverting voltage of the inverter was $V_I = 2.41$ V and $V_O = 2.81$ V before the stress. It was observed that the value of the inverting point of the voltage transition characteristic shifted to $V_I = 2.41$ V and $V_O = 2.51$ V after a stress of 18 h.

Lifetime Prediction

In order to allow a prediction of device lifetime in real life, stress levels from results obtained under actual stress conditions must be used. With such results, empirical models for hot-carrier degradation and several extrapolation laws to calculate the lifetime have been developed. However, the proposed model combines a hot-carrier degradation model and lifetime prediction model into a single model [34, 37–41]. Lifetime predictions for MOS transistors have been performed using the criteria given in the literature [37]. They can reach 10% of the lifetime criteria [37] for hot carriers in DC stress applications in 10 years or less. One year in static conditions is

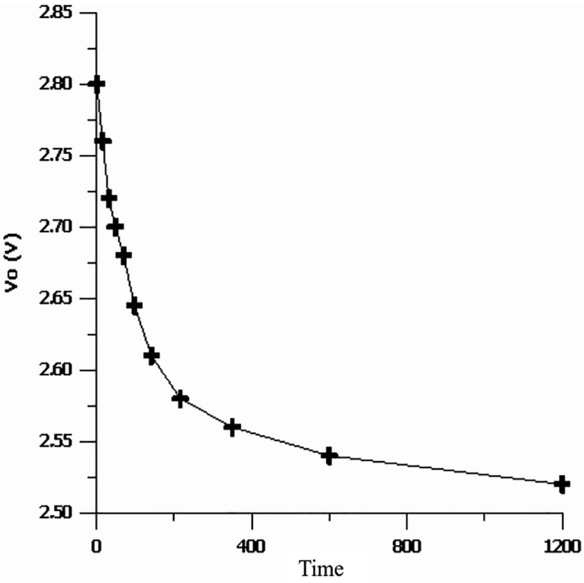


Fig. 3.10 Change in the inverting voltage of the CMOS inverter with time [1]

equivalent to 10 years in real operating conditions, in an analog application (Fig. 3.10).

Lifetime prediction calculations for MOS transistors were performed with respect to the logarithmic method using the functions of the proposed methods and 10% drain current criteria, which are given in the literature [37]. Lifetime prediction results obtained by calculations for different operating conditions can be seen in Table 3.4. Similarly, a function for the change in the output characteristic of the CMOS inverter with lifetime prediction was obtained and it was calculated to be 1.52×10^3 min.

Concluding Remarks

In this part, a demonstration on an application example of CMOS inverter is performed. In CMOS inverters, the change of the current and threshold voltage of the transistors has an important effect on the value of the inverting voltage of the circuit. Lifetime prediction calculations for MOS transistors were performed with respect to the logarithmic method using the functions of the proposed methods and 10% drain current criteria, which are given in the literature.

Table 3.4 Calculated lifetime prediction of PMOS transistors for different channel lengths [1]

	PMOS Predicted liftime (min)	
Channel length (μm)	Subthreshold region	Inversion region
$L = 1.5$	2.16×10^3	3.76×10^6
$L = 2$	6.83×10^3	2.10×10^7
$L = 3$	4.00×10^4	6.10×10^8

Statistical Investigation of Symmetrical CMOS OTA Degradation

Basic Concept

Today's manufacturers are facing new pressures to develop highly sophisticated products to match rapid advances in technology, intense global competition, and increasing customer expectations. As a result, manufacturers must produce components in record time, while improving productivity, reliability, and overall quality of the component. "It is a significant challenge to design, develop, test, and manufacture highly reliable products within short turn times and within the stringent conditions, imposed by both internal and external circumstances [42]. Estimating the time-to-failure distribution or long-term performance of components of high reliability products is particularly difficult. Most modern products are designed to operate without failure for several years. Thus few of such units will fail or degrade to a significant amount in a test of any practical length based on normal use conditions. For example, during the design and construction of a communication satellite, there may be only 6 months available to test the components which are meant to be in service for 15–20 years. The components used in submarine cables are often required to operate for 25 years under the sea. Very few test units are available that will actually reflect the life profiles of these components. For these reasons, accelerated tests (ATs) are used widely in manufacturing industries, particularly to obtain timely information on the reliability of products [43, 44]. To meet increasing competition, get products to market in the shortest possible time, and satisfy heightened customer expectations, products must be made more robust and fewer failures must be observed in a short development period. In this circumstance, assessing product reliability based on degradation data at high stress levels becomes necessary. This assessment is accomplished through accelerated degradation tests (ADT). These tests involve over stress testing in which instead of life product performance is measured as it degrades over time [45].

The failures of many manufactured products are caused by certain degradation mechanisms. For a particular unit of such a product, degradation measurements can be made over time. Such degradation measurements can be used to make inference on the lifetime distribution of the product. Degradation analysis for reliability has

attracted considerable attention of statisticians, and engineers in recent years [46–50].

Major advantage of performing reliability analysis based on performance (e.g., voltage, current, and dielectric) degradation data is that it relates the reliability analysis to the physics of failure mechanism. Many papers have been written on reliability degradation modeling research and applications [42–49]. Basically, there are two types of reliability degradation modeling being widely used: the degradation path curve approach and the graphical approach. The degradation path curve approach is based on the trajectory (the so-called path curve) of performance degradation versus time [43–45]. This approach requires a known physics model of degradation. If a physics model is not available, a statistical method is needed to obtain the path curve. In general, the path curve is expressed as a function of time, containing both constant and random coefficients. Numerical estimation of the parameters of a multivariate distribution function is required and is usually computationally intensive. The graphical approach is widely used in practice [33, 46–57]. It is based on statistical models. The mean time expected to the first failure of a piece of equipment. It is a statistical value and is meant to be the mean over a long period of time. For constant failure rate systems, the mean time to failure (MTTF) is the inverse of the failure rate or can be calculated using the following equation:

$$\mathrm{MTTF} = \int_0^\infty tf(t)\,\mathrm{d}t \tag{3.3}$$

In this section, transistor lifetimes are calculated using the degradation path curve approach. After that, lifetimes are investigated statistically. Probability density function, reliability function, and failure rate curves are obtained and MTTF calculated.

Statistical Method

The object of primary interest is the reliability function, conventionally denoted R, which is defined as:

$$R(t) = \Pr(T > t) \tag{3.4}$$

where t is the some time, T is the time of death, and "Pr" stands for probability. Related quantities are defined in terms of the survival function. The lifetime distribution function, conventionally denoted F, is defined as the complement of the reliability function,

$$F(t) = \Pr(T \le t) = 1 - R(t) \tag{3.5}$$

and the derivative of F (i.e., the density function of the lifetime distribution) is conventionally denoted f,

$$f(t) = \frac{\partial}{\partial t} F(t) \tag{3.6}$$

f is sometimes called the event density; it is the rate of death or failure events per unit time. The failure rate (hazard function), conventionally denoted λ, is defined as the event rate at time t conditional on survival until time t or later,

$$\lambda(t)\partial t = \frac{f(t)\partial t}{R(t)} = -\frac{R'(t)\partial t}{R(t)} \tag{3.7}$$

Change in output current is used for the degradation data. The behavior of the change in output current fits the power curve and logarithmic curve in the literature [43].

Results

Accelerated life test is applied to five same symmetrical CMOS OTAs as shown in Fig. 3.11. OTAs are produced by TUBITAK (Turkish Scientific and Technical Research Council) Laboratories with 3 μ technology [11, 12]. Power curve is presented as $Y = B \cdot t^A$ and logarithmic curve is as

$$Y = A \cdot \ln(t) + B \tag{3.8}$$

Degradation results are fitted both power and logarithmic curves for five experiment results, illustrated in Figs. 3.12 and 3.13.

In Table 3.5 A and B, coefficients are seen for power and logarithmic curve. For each curve, error mean and the variance is calculated using MATLAB. Results are given in Table 3.6.

It is seen that variances of the logarithmic curves are smaller than the power curves. Thus, logarithmic curves are used for the change in the degradation data. Lifetimes of the OTA's are calculated by using the logarithmic curve equations and %10 lifetime criteria [10]. Results are given in Table 3.7.

Probability density function of the OTA's lifetimes is extracted. Firstly, it is assumed that the pdf of the lifetime is normal, lognormal, Weibull 2, Weibull 3, gamma distributions. Log-likelihood values are calculated with Weibull++ 7 program and −66.26, −65.18, −65.56, −63.52, −65.69 values are handled, respectively. It is seen that distribution is Weibull-3 distribution and shown in Fig. 3.14. For Weibull-3 distribution pdf, reliability and the failure rate equations are shown in Eqs. 3.5–3.7. These equations are can be extracted from Eqs. 3.1–3.4. The Weibull parameters are given in Table 3.8.

The pdf equation is:

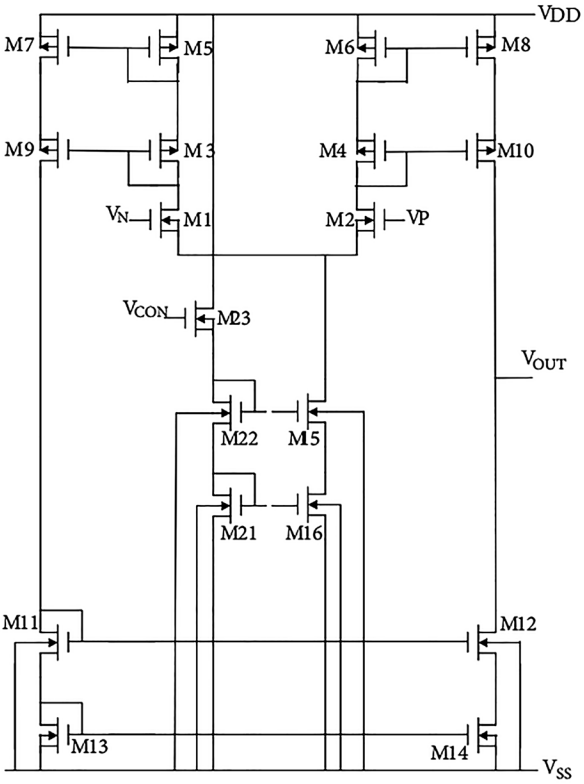


Fig. 3.11 OTA realization used in experiments [33]

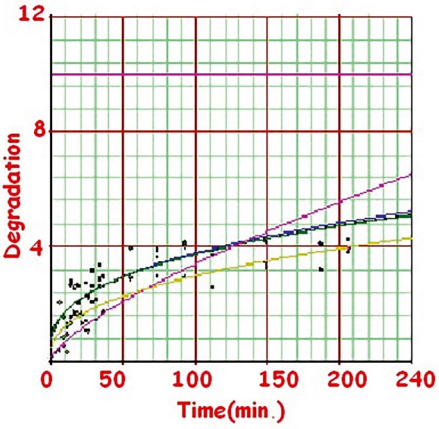


Fig. 3.12 Power curve fitted to degradation data [33]

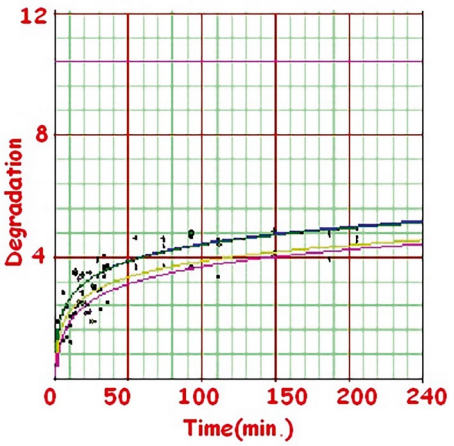


Fig. 3.13 Logarithmic curve fitted to degradation data [33]

Table 3.5 A and B coefficients for curves [33]

	B	A
	Power curve coefficients	
OTA1	0.8019663441	0.3539553012
OTA2	0.8137570676	0.3473666146
OTA3	0.8299310578	0.3428769927
OTA4	0.1489591538	0.7131710871
OTA5	0.5135829766	0.4017473705
	Logarithmic curve coefficients	
OTA1	−0.0117	0.8547874243
OTA2	0.0197	0.8377821571
OTA3	0.0454	0.8331976069
OTA4	−0.8245080446	0.8588552508
OTA5	−0.3249243575	0.7891767497

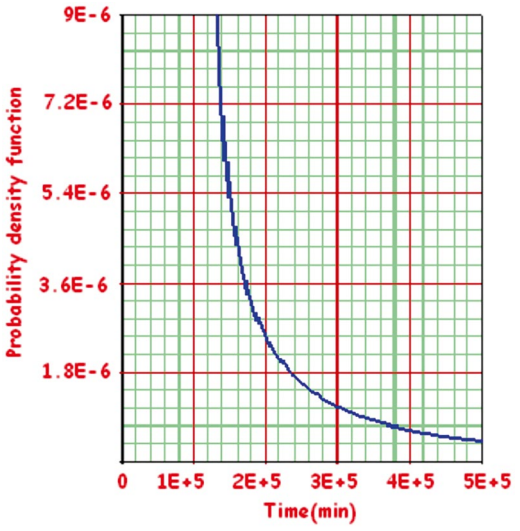


Fig. 3.14 Probability density function of the OTA lifetime [33]

Table 3.6 Mean and variance of error of the power and logarithmic curves [33]

	Variance	Mean
	Power curve	
OTA1	0.2312	0.0322
OTA2	0.2250	0.0340
OTA3	0.2291	0.0359
OTA4	0.7774	−0.0504
OTA5	0.4461	0.1458
	Logarithmic curve	
OTA1	0.1940	0.00002120
OTA2	0.1969	−0.00000724
OTA3	0.2029	0.00000084
OTA4	0.1910	0.00000075
OTA5	0.4649	0.00000203

Table 3.7 CMOS OTA's lifetime [min] [33]

	Lifetime (min)
OTA1	122,085.81
OTA2	149,159.56
OTA3	154,425.52
OTA4	297,572.66
OTA5	480,776.75

Table 3.8 Weibull 3 parameters [33]

Weibull parameters	
Shape parameter β	0.860500434
Scale parameter η	117,837.2812
Location parameter γ	113,318.9452

$$f(t)=\left(\frac{\beta}{\eta}\right)\left(\frac{t-\gamma}{\eta}\right)^{\beta-1}.\exp\left[-\left(\frac{t-\gamma}{\eta}\right)^{\beta}\right] \tag{3.9}$$

Reliability equation:

$$R(t)=\exp\left[-\left(\frac{t-\gamma}{\eta}\right)^{\beta}\right] \tag{3.10}$$

The failure rate equation:

$$\lambda(t)=\left(\frac{\beta}{\eta}\right)\left(\frac{t-\gamma}{\eta}\right)^{\beta-1} \tag{3.11}$$

The lifetime is calculated as 2.4×10^5 min using the density function of the lifetime distribution. Reliability function of the CMOS OTA is shown in Fig. 3.15. The failure rate (or the hazard function) is shown in Fig. 3.16.

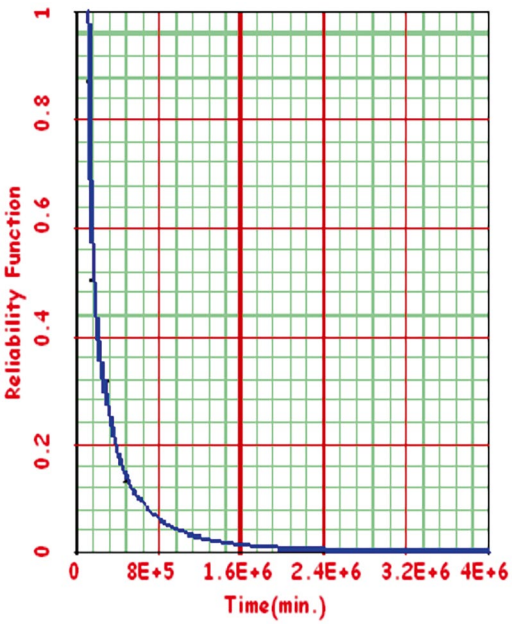


Fig. 3.15 Reliability function of the CMOS OTA [33]

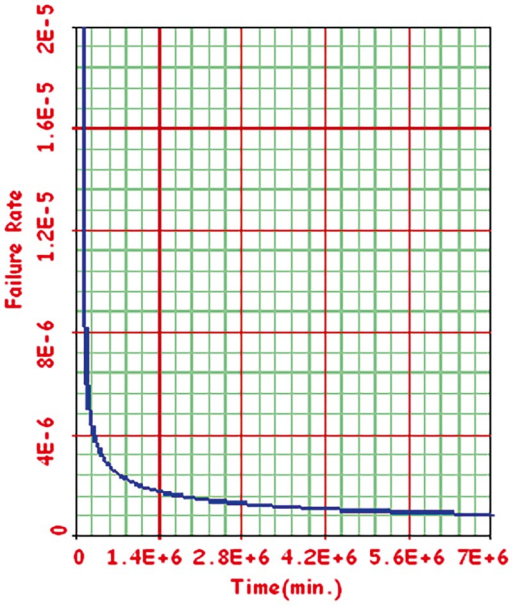


Fig. 3.16 Failure rate curve of the CMOS OTA [33]

Using the failure rate curve, failure rate of the CMOS OTA could be calculated for example 6×10^6 min operation (failure rate is constant around). From Fig. 3.16, failure rate is 4.22×10^{-6} failures/min. It says 4.22 failures are estimated for every million minutes of operation. The mean time to failure (MTTF) is inverse of the failure rate and the MTTF is 1,000,000/4.22 = 236,966.82 min.

Concluding Remarks

Symmetrical CMOS OTA degradation was investigated by using the degradation path curve and statistically in this study. Output current is released as degradation data and logarithmic curves exhibited to the changes in degradation data better than the power curves. Lifetimes are calculated and used for the statistical investigation. Probability density function, reliability function, and the failure rate curves are presented. Failure rate and the MTTF are calculated. This work presents a degradation investigation method for any electronic devices.

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Chapter 4
On the Degradation of OTA-C-Based CMOS Low-Power Filter Circuits for Biomedical Instrumentation

Basic Concept

The trend of microelectronic products in the biomedical field is toward higher functionality and miniaturization. As with other electronic devices, the miniaturization of biomedical devices is limited by the reliability of the manufactured product at a desired circuit density. Biomedical device failure or the disorder of biomedical device function during diagnosis and treatment processes may have extremely negative effects. Thus, in order to determine the ultimate performance, the reliability must be modeled for specific operating condition [1–13]. Circuits needed for processing of biological signals are typically low-power and small-sized building blocks. The main features of biological signals are their low-amplitude and low-frequency range. Most biomedical devices monitor patients all day long, and, therefore, such devices must have low-power dissipation. A typical low-power biomedical device can be composed of complementary metal-oxide semiconductor (CMOS) circuits, operating in the subthreshold (weak inversion) region. CMOS circuits such as operational transconductance amplifiers (OTAs), operating in the subthreshold region, introduce a versatile solution for the realization of low-power building blocks [14–17]. OTAs provide highly linear electronic tunability of their transfer gain (G_m) and require just a few or even no resistors for their internal circuitry. The use of circuits composed of operational transconductance amplifiers and capacitors (OTA-Cs) has been demonstrated to be potentially advantageous for the synthesis of monolithic analog building blocks.

The most important advantage provided by OTA-C filters operated in the subthreshold region is the possibility of constructing filters with small capacitance values of the order of several pFs, which cannot be obtained by conventional active-filter techniques, where capacitance values of the order of several μF are necessary for this frequency range. Owing to the small capacitance values, the complete filter circuit is realizable on a single very-large-scale integration (VLSI) chip using the

H. Kuntman et al., *Reliability of CMOS Analog ICs*, Analog Circuits and Signal Processing, https://doi.org/10.1007/978-3-031-85455-2_4

CMOS technology [17]. However, hot-carrier-induced degradation is the most important factor that affects the reliability of the miniaturized CMOS circuits in electrical operating conditions. Degradation phenomena influence the circuit performance parameters, and, as a result, changes in the output current and in the filter cutoff frequencies are observed. Therefore, circuit performance parameters create great interest because of their important role in device reliability [18]. Several works are available in the literature that were performed on the reliability of CMOS analog circuits [19–21].

"Hot carrier" is a phenomenon in solid-state electronic devices where an electron or a hole gains sufficient kinetic energy to overcome a potential barrier necessary to break an interface state. The term "hot" refers to the effective temperature used to model the carrier density, not to the overall temperature of the device. Since the charge carriers can become trapped in the gate dielectric of a metal-oxide semiconductor (MOS) transistor, the electrical characteristics of the transistor can be permanently changed. Hot-carrier injection is one of the mechanisms that adversely affect the reliability of the semiconductors of solid-state devices [22]. Some works have been performed for the modeling of hot-carrier degradation in MOS transistors and for its inclusion in a simulation program with integrated circuit emphasis (SPICE) transistor model, using physical equations [21, 23] or statistical equations [19, 24–27], based on experimental observations. In a previous work, hot-carrier-induced degradation of CMOS OTA electrical parameters, such as transconductance G_m and maximum output current I_{Omax} were investigated via accelerated laboratory measurements. Furthermore, a degradation model was proposed for the reliability of CMOS OTAs [18]. Investigations show that there is a need of determining the most degraded transistors in a CMOS circuit, such as filters for biomedical instrumentation, to enable the designer to easily guess the changes in the active device's performance through computer simulations and to specify a reliable operation [28, 29].

In this section, hot-carrier-induced degradation of an electroencephalogram (EEG) band-pass filter structure composed of symmetrical CMOS OTAs is investigated. In this context, we propose a degraded transistor-based circuit degradation simulation method that is applicable to any CMOS device. The proposed method is based on the determination of the degraded transistors in the structure under stress conditions and includes the use of a degraded transistor model to adapt the experimental results of the transistor degradation to the simulation. In our study, we first simulated the symmetrical CMOS OTA degradation, considering the output current. Furthermore, to demonstrate the accuracy of the proposed method, the changes in the cutoff frequencies of the first and second-order low-pass filters, composed of symmetrical CMOS OTAs, were investigated. We then compared the experimental results in our earlier study [18] (described at the second part of this chapter) with the simulation results in this study, and as the experimental and simulation results were found to be in good agreement, the hot-carrier-induced degradation of the EEG band-pass filter structure was investigated using the proposed method.

Method

The symmetrical CMOS OTA structure intended for biomedical applications is shown in Fig. 4.1. It was produced by the Scientific and Technological Research Council of Turkey (TUBITAK YITAL) and is composed of 11 N-type MOS (NMOS) and 8 P-type MOS (PMOS) transistors. The channel length of all of the transistors is 3 μm and the channel widths of the transistors are 5 and 10 μm for the NMOS and PMOS transistors, respectively [29–34].

We propose a degraded transistor-based circuit degradation simulation method that is applicable to any CMOS biomedical device. The proposed method is based on determining the degraded transistors in the structure under stress conditions. First, the symmetrical CMOS OTA degradation is investigated by considering the basic performance parameters transconductance G_m and output current I_O for a control voltage of $V_{CON} = -3$ V. There are filter applications for the human EEG that provide a rich picture of the electrical activities of the brain, which is one of the most important biological signals [35]. In our earlier study, symmetrical CMOS OTA degradation was identified experimentally. DC stress voltage was chosen as

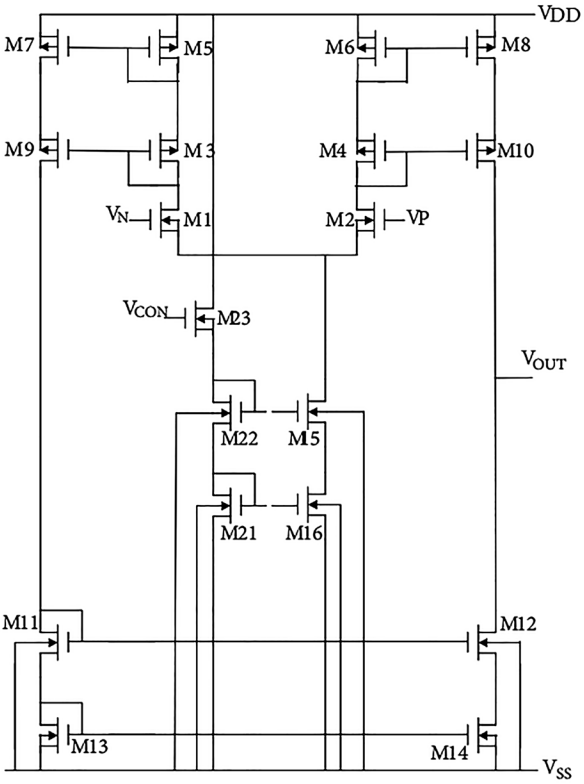

Fig. 4.1 Symmetrical CMOS OTA structure [34]

5 V and was applied from the V_{CON} and V_n terminals to the OTAs for a time period of 4 h. During the degradation process, changes in the output current versus the input voltage curves were recorded at 15-min intervals. The measurements were performed at the Electronics Laboratory of the Electronics and Communication Engineering Department of Istanbul Technical University using the HP 4155 parameter analyzer [16].

The type of the stress can be chosen as AC; however, note that it is easier to apply the DC stress and it is assumed that many electronic devices degrade under DC stress during normal operating conditions. There are four commonly encountered hot-carrier injection mechanisms: (1) the drain avalanche hot-carrier injection, (2) the channel hot electron injection, (3) the substrate hot electron injection, and (4) the secondary generated hot electron injection. In our study, the channel hot electron injection mechanism occurs due to the stress conditions [33]. To determine the degraded transistors, the lateral electrical field values in the channel have to be calculated under DC stress conditions. Hence, if the lateral electrical field increases, the hot-carrier effect occurs. This effect was first observed by Ryder and Shockley at fields of 10^3 V/cm [33, 34]. Electrical fields of about 10^4 V/cm (as in our study) are agreeable as relatively moderate fields [33, 34], and the hot-carrier effect surely occurs [32]. The drain-source voltages (V_{DS}) of all of the transistors in the symmetrical CMOS OTA are obtained under DC stress conditions with PSpice, and lateral electrical field values are calculated using Eq. (4.1),

$$E_{lat} = \frac{V_{DS}}{L} \tag{4.1}$$

where L is the channel length. The drain-source voltages and lateral electrical field values of all of the transistors in the symmetrical CMOS OTA under stress conditions are presented in Table 4.1.

The drain-source voltages and lateral electrical field values of all of the transistors given in Table 4.1 show that the hot-carrier-induced degradation occurs in

Table 4.1 Drain-source and lateral electrical field values of the transistors in the symmetrical CMOS OTA's under stress conditions, bold values indicate the most influenced transistors

Transistor	V_{DS} (V)	$E_{Lateral}$ (10^4 V/cm)	Transistor	V_{DS} (V)	$E_{Lateral}$ (10^4 V/cm)
M1	0.39	0.13	**M11**	**3.27**	**1.09**
M2	2.5	0.83	M12	0.17	0.05
M3	**−3.23**	**−1.08**	M13	2.675	0.89
M4	−2.18	−0.72	M14	0.345	0.11
M5	**−3.23**	**−1.08**	M15	0.94	0.31
M6	−2.18	−0.72	M16	2.19	0.73
M7	−2.74	−0.91	M21	**3.11**	**1.04**
M8	−2.21	−0.73	M22	**3.77**	**1.25**
M9	−1.31	−0.43	M23	**3.11**	**1.04**
M10	**−7.26**	**−2.42**			

transistors M_3, M_5, M_{10}, M_{11}, M_{21}, M_{22}, and M_{23}. The degraded M_3, M_5, and M_{10} transistors are PMOS transistors and the M_{11}, M_{21}, M_{22}, and M_{23} transistors are NMOS transistors. After determining the degraded transistors, there is a need for a degraded transistor model to perform the experimental hot-carrier-induced transistor degradation results for the simulation. For this purpose, a current-controlled current source is connected between the drain and source terminals of the MOS transistor. The degraded transistor model is shown in Fig. 4.2 [20–22, 33, 34].

In Fig. 4.2, ΔI_D represents the change in the output current of the transistor with the effect of the hot-carrier-induced degradation. In this study, the experimental results of the transistor degradation were taken from [33–36], and the degradation results of the NMOS-PMOS transistors operating in the subthreshold are shown in Fig. 4.3. BSIM3 parameters are used in the simulations. The degradation of the symmetrical CMOS OTA is simulated using the proposed method, and the change in the OTA's output current versus the V_{in} curve is shown in Fig. 4.4 for before (fresh) and after the stress.

It is seen in Table 4.2 that the experimental results and the proposed simulation method results are close to each other. We took the experimental results from our earlier study [33–36]. The transconductance of the symmetrical CMOS OTA (G_m) is the most important characteristic parameter, and we also investigated the hot-carrier-induced degradation of the symmetrical CMOS OTA transconductance using the proposed method. We compared the proposed degradation simulation method results with the experimental and "macromodel-based" degradation simulation results from our earlier study [33–36]. The results obtained are shown in Fig. 4.5. In addition, a further curve denoted as "all transistor" is also shown in Fig. 4.5, where all of the transistors in the symmetrical CMOS OTA are assumed to be degraded under DC stress conditions.

It is obvious from Fig. 4.5 that the results of the proposed transistor-based simulation method are in good agreement with the experimental results, whereas the simulation results performed assuming that all of the transistors are degraded in the OTA structure strongly differ from the experimental results. This tells us that when a CMOS device is under stress, not all of the transistors in the device are affected.

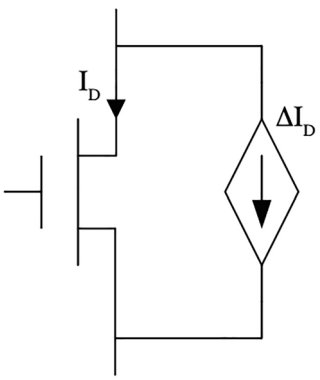

Fig. 4.2 Degraded transistor model in the symmetrical CMOS OTA structure [34]

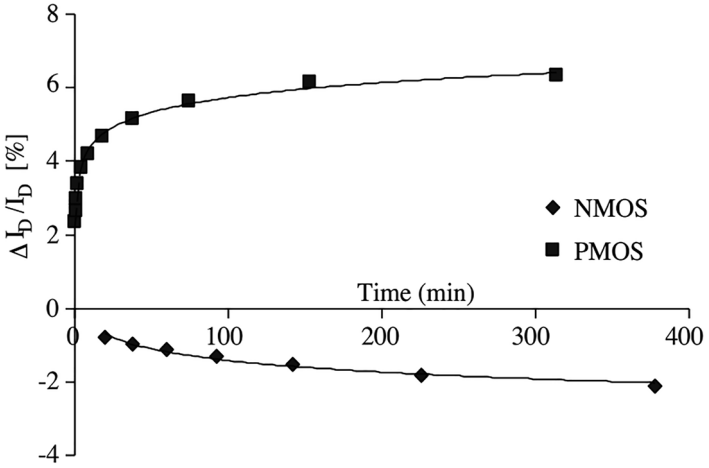

Fig. 4.3 Degradation results of the NMOS-PMOS transistors operating in the subthreshold region [34]

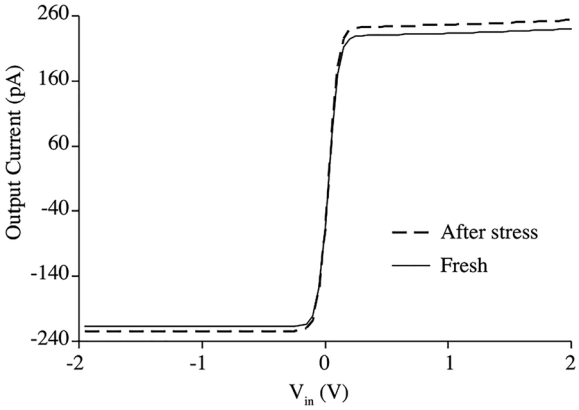

Fig. 4.4 Plot of the symmetrical CMOS OTA output current against V_{in} ($V_{con} = -3$ V) [34]

Therefore, the designer has to determine which transistors are degraded in an active circuit. From this point of view, we investigated the degradation of the first- and second-order low-pass filters, which are composed of symmetrical CMOS OTAs, to demonstrate the accuracy of the proposed method. The first- and second-order low-pass OTA-C filters shown in Fig. 4.6 were performed in PSpice using the proposed method.

The first-order and second-order low-pass filter curves are shown in Figs. 4.7 and 4.8, respectively, before (fresh) and after the stress. The change in the cutoff frequency is 4.23% for both the first- and second-order low-pass filters using the proposed method. In Table 4.3, the change in the cutoff frequencies of the filters is shown for the experiments and the simulation. It is seen that the cutoff frequency change is in good agreement with the experimental results.

Table 4.2 Change in the output current of the symmetrical CMOS OTA [34]

	Simulation with proposed method	Experimental
$\Delta I_{omax}/I_{omax}[\%]$	4.21	4.2

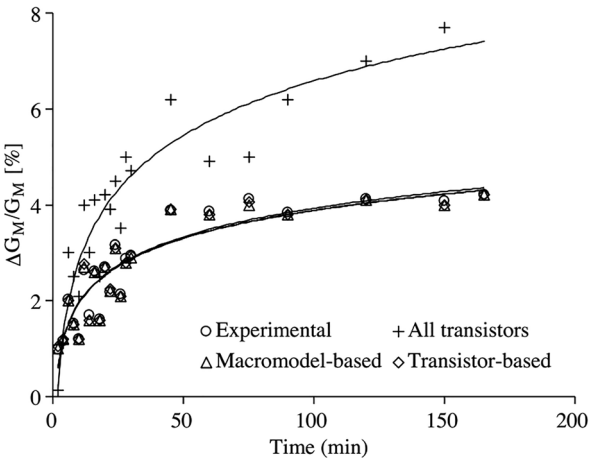

Fig. 4.5 Dependence of the symmetrical CMOS OTA transconductance on stress time [34]

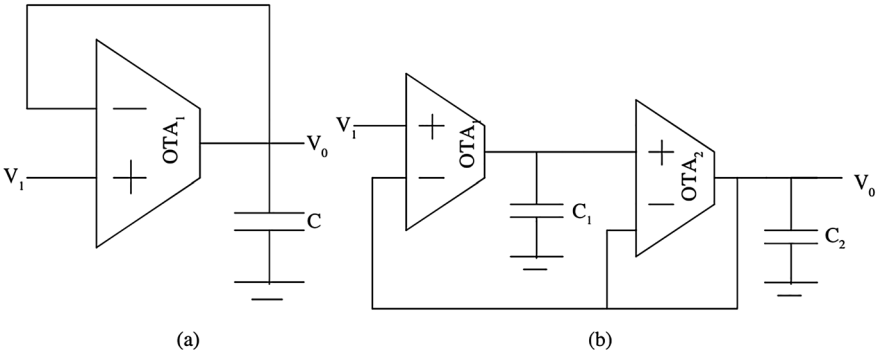

Fig. 4.6 First-order (**a**) and second-order (**b**) low-pass filter structures [34]

Application Example of EEG Filter

OTA-C-based filter structures are widely used in the biomedical field and there is much relevant research in the literature. Hereafter, degradation of the OTA-C band-pass filter to process EEG signals is investigated using the proposed degradation simulation method. The filter used in this study was proposed by Duzenli et al. [35], whereby normal subjects usually exhibit α (8–12 Hz), β (13–40 Hz), θ (4–8 Hz), and δ (1–4 Hz) activities. Signal α provides information about the patient's coma situation. The filter structure is shown in Fig. 4.9. The major

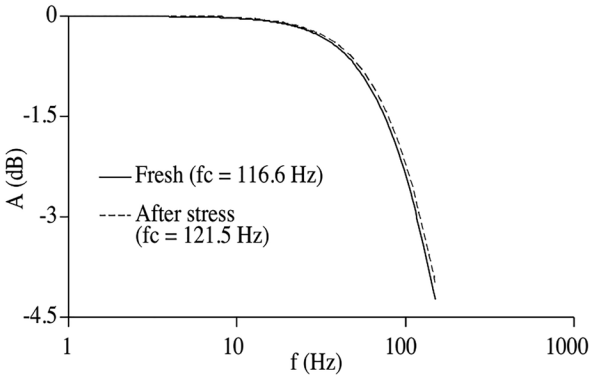

Fig. 4.7 First-order low-pass filter frequency curve before and after the stress [34]

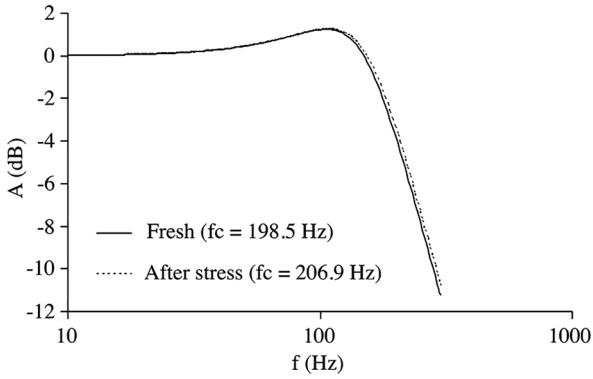

Fig. 4.8 Second-order low-pass filter frequency curve before and after the stress [34]

Table 4.3 Change in the cutoff frequencies of the filters [34]

$\Delta f_c/f_c$ [%]		
	Simulation with proposed method	Experimental
First-order low-pass filter	4.23	4.4
Second-order low-pass filter	4.23	4.6

advantage of this band-pass filter is the possibility of constructing EEG band filters with small capacitance values of the order of 25–400 pF, which cannot be obtained by conventional active-filter techniques where capacitance values of the order of several μF are necessary for this frequency range. This is achieved by the use of CMOS OTA structures operating in the subthreshold region. Owing to the small capacitance values, the complete filter circuit is realizable on a single VLSI chip using the CMOS technology. The integrated circuit (IC) realization of the complete filter will enable the user to implement the circuit on implantable biotelemetric applications where low-power consumption and small-sized capacitors are required [35]. There are six OTAs in the structure and we can also investigate the degraded

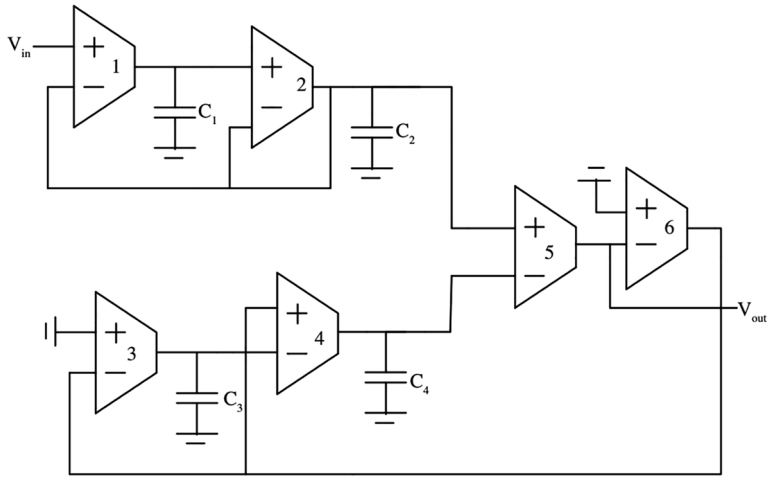

Fig. 4.9 Band-pass filter structure [35]

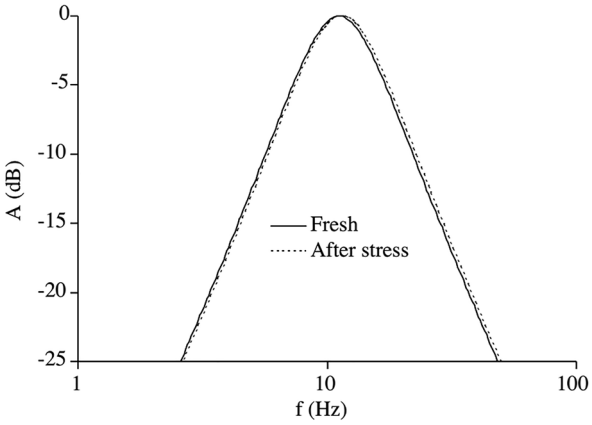

Fig. 4.10 Band-pass filter operating in the α band frequency curve before and after the stress [34]

OTA number effects in a structure. The frequency response of a filter operating at the α band is shown in Fig. 4.10 before and after the stress. We assumed that all of the OTAs in the structure are degraded and used experimentally degraded OTA results. We simulated the filter using PSpice before and after the degradation. The band-pass filter operates at an interval of 8–12 Hz before the stress. After the stress, the lower cutoff frequency shifts to 8.21 Hz and the uppercut off frequency shifts to 12.31 Hz. In other words, the lower cutoff frequency changes by 2.66% and the upper cutoff frequency changes by 2.61%. These changes result in errors in the diagnosis, which affects human health. On the other hand, the output current of the filter increases by 6.9%.

Concluding Remarks

In this part, we proposed a transistor-based circuit degradation simulation method to investigate the degradation in CMOS low-power biomedical circuits. The method depends on the determination of degraded transistors in any CMOS circuit using PSpice simulations under certain stress conditions at the first step. After that, at the second step, the performance of the degraded circuit is simulated using the degraded transistor model to obtain the influence of the degradation on the overall performance of the application circuit. The accuracy of the method is demonstrated by the degradation of the first- and second-order low-frequency filter examples suitable for biomedical applications. Furthermore, we demonstrated the advantage provided by the proposed method on the degradation of an EEG band-pass filter composed of symmetrical CMOS OTAs under DC stress conditions. The proposed degradation simulation method results and the experimental results were found to be in good agreement. It can be easily observed that hot-carrier-induced degradation has negative effects on the EEG band-pass filter. The proposed method can provide the IC designer with new possibilities for estimating the reliability of CMOS-based biomedical topologies operating in the subthreshold region. Furthermore, the method proposed is applicable to any CMOS device, such as operational amplifiers, current conveyors, and multipliers.

On the Reliability of Symmetrical CMOS OTA Operating in Subthreshold Region, a Reliability Macromodel

Basic Concept

As a result of the decrease in gate oxide thickness and increase in the electrical fields, the generation of hot carriers becomes a serious problem in current-day CMOS technology. Therefore, the transistor produced influence the lifetime of the circuit and thus needs to be analyzed and calculated during the design of circuit [36]. The reliability of a system is defined as the probability that it will perform its required function under stated conditions for a stated period of time. Rapid changes in the technology, shorter periods in product development and higher reliabilities of products make accelerated life tests even more useful and important in the industry of today. Accelerated life tests are used to obtain timely information on the times to failure distributions of components and systems [37]. Hot-carrier-induced phenomena influences transistor performance parameters such as threshold voltage and drive currents in all operating regimes; it therefore continues to create great interest because of its important role in device reliability. Several works were performed for investigation of hot carrier effect on the performance of NMOS and PMOS transistors and for digital and analog cases [28, 38, 39]. CMOS circuits such as OTAs (operational transconductance amplifiers) operating in the subthreshold (weak

inversion) region introduce a versatile solution for the realization of low-power VLSI building blocks [28, 39]. In this paper, hot-carrier-induced degradation of CMOS OTA electrical parameters such as transconductance G_m and maximum output current I_{Omax} are investigated by accelerated laboratory measurements. A degradation model is proposed for reliability of CMOS OTA. As a second step, to demonstrate that the model proposed is independent of the realization technology, the circuit is also investigated by SPICE simulations using the observation based hot carrier degradation models for MOS transistors available in the literature [28, 37–39] where a different CMOS technology is used for realization.

Measurements

Operational transconductance amplifiers (OTAs) are versatile building blocks for many applications such as filters, oscillators, and so on. OTA transconductance and maximum output current I_{OMAX} are two important parameters determining the behavior of OTA-based topologies. Accelerated measurements are performed for the investigation of hot-carrier-induced degradation on these electrical parameters of CMOS OTAs. The experiments were performed on OTAs produced by TUBITAK (Turkish Scientific and Technical Research Council) Laboratories [28, 37–39]. For OTA degradation, the biasing circuit shown in Fig. 4.11 is used. Symmetrical CMOS OTA structure is illustrated previously in Fig. 4.11.

On the other hand, the rapid increasing use of battery-operated portable equipment in application areas such as telecommunications and medical electronics increases the importance of low-power and small-sized circuits realized with VLSI technology.

Degradation is applied to the OTAs for a time period of 4 h. During the degradation process, changes in the output current vs. input voltage curves are recorded with 15 min intervals. Measurements are performed in Electronics Laboratory of Electronics and Communication Engineering Department of I.T.U. (Istanbul Technical University) by using the parameter analyzer HP 4155.

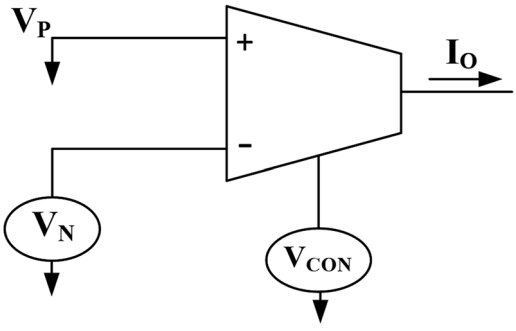

Fig. 4.11 OTA measurement mechanism for degradation [16]

Experimental Results

An OTA measurement mechanism is illustrated in Fig. 4.11, where two OTA samples are degraded. The I_O-V_{in} curve obtained for CMOS OTA operating in subthreshold region before and after the stress is shown in Fig. 4.12. Using the experimental measurement results, change in OTAs maximum output current I_{OMAX} vs. time curve is also extracted and shown in Fig. 4.13. The change in transconductance, the most important characteristic parameter, is extracted according to experimental measurement results. Change in transconductance is investigated for subthreshold region. Result is shown in Fig. 4.14.

Lifetime Estimation for CMOS OTA

Several models for the lifetime estimation of MOS transistors are available in the literature. One useful model is proposed by Takeda-Suzuki which calculates the transistor lifetime as a function of the bias voltage and gate length [28]. Starting from Takeda-Suziki model, we propose the following equation for modeling of the percentage change in the OTA transconductance G_m with the stress time:

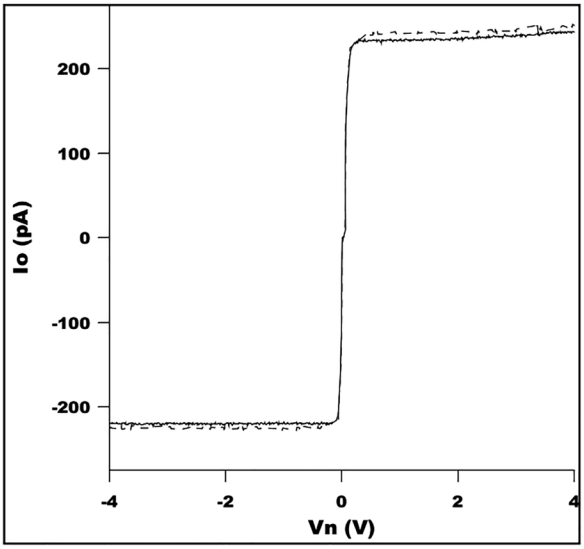

Fig. 4.12 Plot of output current against V_N. Control voltage V_c = –3 V. Before the stress (dark line), after the stress (dashed line) [16]

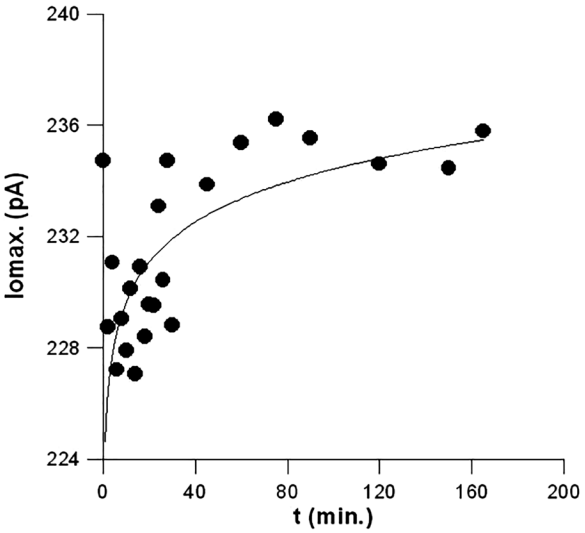

Fig. 4.13 Maximum output current I_{Omax} vs. time for subthreshold operating region [16]

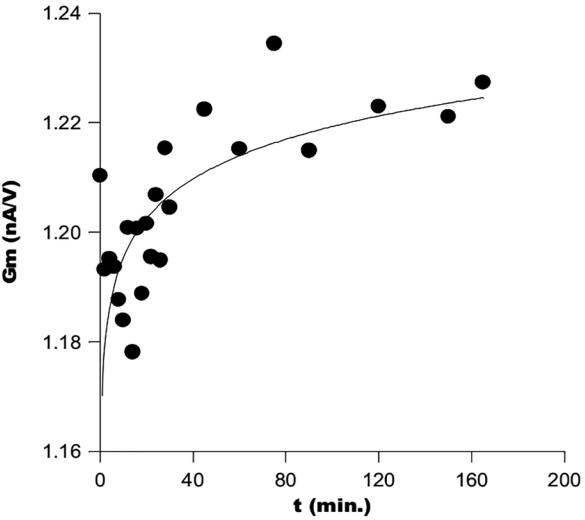

Fig. 4.14 OTA transconductance G_{m} vs. time (• measurement results) (fitted curve) [16]

$$\left(\frac{\Delta G_{\mathrm{m}}}{\Delta}\right)\% = A \cdot t^{n} \tag{4.2}$$

where A and n are the empirical model parameters [28].

The lifetime of the CMOS OTA can be extracted by using the curve shown in Fig. 4.14. Applying curve fitting methods, it is observed that the change in the transconductance G_m with the stress time illustrates a logarithmic curve. Thus, it can be written as follows:

$$\ln\left(\frac{\Delta G_m}{G_m}\right) = n \cdot \ln t + A \tag{4.3}$$

Plot of $\ln(\Delta G_m/G_m)$—$\ln(t)$ yields a straight line. Applying this to Fig. 4.5, we obtain $n = 0.00860117$ and $A = 1171.94$. For a change of 10%, the lifetime [28–36] of the CMOS OTA is calculated as $\tau = 4.6 \times 10^7$ s. In this respect, Eq. (4.3) can be used to estimate the influence of the hot carrier degradation on the performance of OTA-based circuit applications which is demonstrated in the following. Furthermore, the dependence of maximum output current I_{Omax} on stress time can be approximated as

$$\ln I_{omax} = a \cdot \ln t + b \tag{4.4}$$

From experimental observations, the quantities a and b can be specified as $a = 0.00890558$ and $b = 5.41608$. For the minimum output current I_{Omin}, $a = -0.00880723$ and $b = -5.35513$. The dependence of the transconductance G_m and the maximum output current I_{Omax} and minimum output current I_{Omin} on stress time can be included into the OTA macromodel [35] as shown in Fig. 4.15, where D_1, D_2, V_{B1}, V_{B2} are used for modeling of current limitation. At the output stage, $f_1(t)$ and $f_2(t)$ can be approximated as

$$f(t) = \ln(V_B) = -\left[c \ln(t) + d\right] \tag{4.5}$$

The quantities c and d can be specified as $c = 0.0200934$ and $d = 0.342241$ for V_{B1} and for V_{B2} $c = 0.020304$ and $d = 0.321061$. Related functions for OTA macromodel are summarized in Table 4.4. The advantages provided by the reliability model proposed is demonstrated on two design examples, namely on first-order and second-order low-pass filters illustrated in Fig. 4.16a, b, where cut off frequency deviation is shown in Fig. 4.17 versus stress time the circuit shown in Fig. 4.16a can

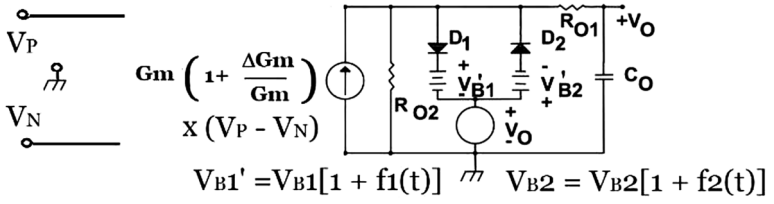

Fig. 4.15 Reliability model for symmetrical CMOS OTA [16]

Table 4.4 Related functions for OTA macromodel [16]

Equation (4.5) evaluations for OTA macromodel
$\ln\left(\frac{\Delta G_m}{G_m}\right) = 0.00860117 \ln t + 1171.94$
$f_1(t) = \ln(V_{B1}) = -[0.0200934 \ln(t) + 0.342241]$
$f_2(t) = \ln(V_{B2}) = -[0.020304 \ln(t) + 0.321061]$

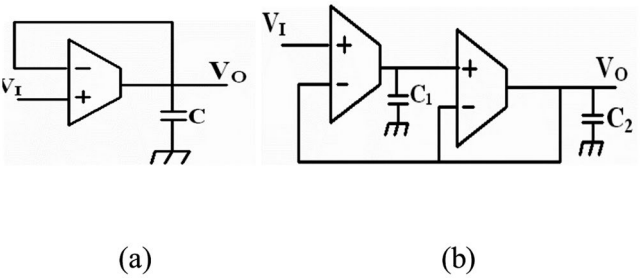

Fig. 4.16 (**a**) First-order low-pass filter, (**b**) second-order low-pass filter [16]

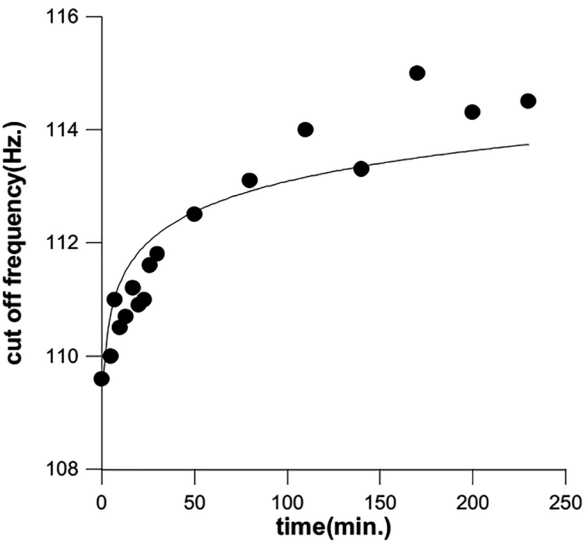

Fig. 4.17 Dependence of cut off frequency on stress time (•experiments) (– theory) [16]

Table 4.5 Estimated and experimental percentage changes on the cut-off frequency of the filters [16]

Cut-off frequency	Before stress (Hz)	After stress (Hz)	Change (%)
First-order low-pass filter			
Estimated	109.6	114.54	4.5
Observed	109.6	114.4	4.4
Second-order low-pass filter			
Estimated	193	202.01	4.67
Observed	193	201.8	4.6

be used as a lossy integrator; the second-order Butterworth type low-pass filter illustrated in Fig. 4.16b is useful for low-power biomedical applications.

From Table 4.5, it can be observed obviously that the estimated values are in good agreement with experimental results. To demonstrate that the method proposed is independent of realization technology, the symmetrical CMOS OTA in Fig. 4.1 is constructed and SPICE simulations were performed using a fully different technology of which hot carrier degradation SPICE models for PMOS and NMOS transistors are available in the literature [28, 35–39]. Several works were performed on the modeling for the influence of hot carrier effect on the MOS transistor performance. Observation-based models were introduced by Düzenli and Kaçar. Düzenli incorporated adequate equations into BSIM model [28, 35–39] to represent the hot-carrier degradation. Recently, Kaçar proposed observation-based statistical models for hot-carrier degradation of MOS transistors. In this work, measurement results given in [28, 35–39] are used for the simulations of n-channel and p-channel transistors *I*–*V* curves in subthreshold region. The results of this work yield an output current percentage of 3.75% for NMOS transistors and 7.22% for PMOS transistors, realized with 1-μm technology SPICE simulations yield similar behavioral results for CMOS OTA as obtained earlier with measurements. Note that similar measurements were also performed on CMOS OTAs operating in strong inversion. It is observed that the influence of hot carriers on behavioral parameters can be neglected for this operation region, therefore this region is not considered in this work.

Concluding Remarks

In this section, hot-carrier-induced degradation of electrical parameters of CMOS OTAs operating in subthreshold region is investigated by accelerated laboratory measurements. Using the experimental observations, a degradation model is proposed for reliability of CMOS OTA. The advantages provided by the degradation model proposed is demonstrated by experiments on design examples of first- and second-order OTA-C filters. The estimated results are found in good agreement with

experiments. The model proposed provides to the IC designer new possibilities to estimate the reliability of OTA-C-based topologies opearting in subthreshold region.

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Chapter 5
Power MOSFET Degradation and Statistical Investigation of the Degradation Effect on DC–DC Converters and Converter Parameters

Electrical over stress-induced power MOSFET degradation and its effects on DC–DC converters were examined in this chapter. Power MOSFETs experimentally operated above normal operating conditions and stress-induced changes in transistor parameters extracted [1]. Switch-mode DC–DC converters are simulated to show degraded power MOSFET effects statistically [2] and effects on converter parameters [3].

Basic Concept

Mobility degradation is a model parameter of particular significance for MOSFET characterization [4]. The fast and accurate modeling of mobility degradation in time models, capable of handling various processes and different gate and dielectric materials, are still needed for simulating today's VLSI/ULSI circuits [5]. New mobility models should, therefore, account for changes in transistor performance over a wide range of process variables [6].

Electrical stress has an important role in MOS device mobility degradation [7]. Electrical stress exposure results in a build-up of oxide charge in the oxide and an increase in interface trap density at the Si–SiO_2 interface.

These physical effects are reflected in the device's electrical characteristics such as decrease in channel length and decrease in carrier mobility in the channel [8, 9].

This section describes a simple and prognostic electrical stress-induced mobility degradation model for MOS transistors. For this purpose, we performed electrical stress experiments on CoolMOS transistors which is a type of power MOSFETs. We determined the stress-induced changes in transistor parameters. We introduced a quantity C_r (mobility decreasing coefficient) which provides accurate model and predict the mobility degradation in time independently from effects of process or

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operational changes such as oxide thickness, substrate doping, and applied voltages on transistor.

Material and Method

Experiments were performed on the CoolMOS transistors SPA08N80C3, in P-TO220-3-31 package in insulated version, produced by Infineon technologies. Their current and voltage ratings are 8 A and 800 V, respectively. The basic quantities of the transistors are given as $W = 1$ µm, $L = 1$ µm, kp = 8.761 A/V^2 by the manufacturer. The cross-section of the CoolMOS transistor is shown in Fig. 5.1.

The four CoolMOS transistors under test are electrically stressed with the gate bias of $V_G = 40$ V DC, where the source and drain were grounded, at ambient temperature, representing electrical stress. DC stress represents the normal operating conditions degradation best. We chose stress voltage such that it will cause high electric field and create traps, short of breaking the gate oxide. We increased the stress voltage step by step to avoid electrostatic discharge. Farnell, PDD3010A is used for DC power supply. Output current is measured by Thurlby 1503, Digital Multimeter.

We recorded the I_D–V_{DS} and I_D–V_{GS} measurements in time intervals during the stress. Corresponding values of threshold voltage were determined by extrapolation of linear parts of transfer characteristics to intersections with V_G axis ($I_D = 0$), while corresponding values of mobility were determined from slopes of linear parts of measured transfer characteristics. The change in channel length was determined from the MOS transistor saturation equation.

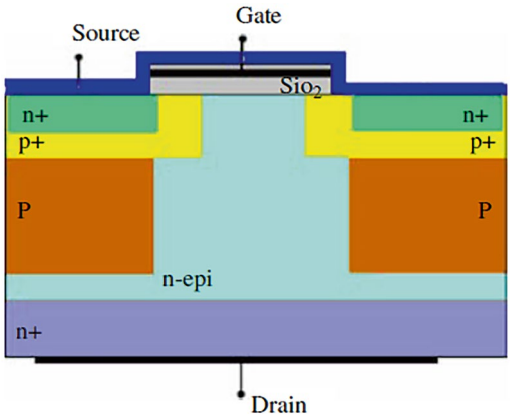

Fig. 5.1 Cross-section of CoolMOS transistor [1]

Electrical Stress Effects on CoolMOS Transistors

We used experimental results and extracted the changes in CoolMOS transistor parameters. We considered the average values of the measurement results. Changes in the output current and threshold voltage are shown in Fig. 5.2a and the changes in the mobility and channel length are shown in Fig. 5.2b.

The output current and the threshold voltage of the CoolMOS transistor are increased after the stress. Mobility and channel length are decreased. In MOS transistors, the trapped charges are accumulated near the drain and result channel length decreases [10]. However, CoolMOS transistor has vertical structure and channel length decreasing region has to be determined.

Channel Length Decrease in CoolMOS Transistors

The schematic representation of the channel length decrease is shown in Fig. 5.3. In CoolMOS transistor, the channel is between the n+ region and n-epi region under the gate. The channel is formed from a pair of half channel ($L/2$) as shown in Fig. 5.3.

It is a well-known fact that MOS transistors operating in saturation region, depletion occurs at the drain side of the channel [10]. In vertical double diffused MOS (VDMOS) structures as CoolMOS transistors, the length of the region under oxide between n-epi and p+ is defined as channel length similar to MOS transistors. In VDMOS according to applied voltage in channel region, the electrical field across the channel region. This electrical field at the edge of the channel is higher. The electrical loads were held by traps and this causes a decrease in channel length.

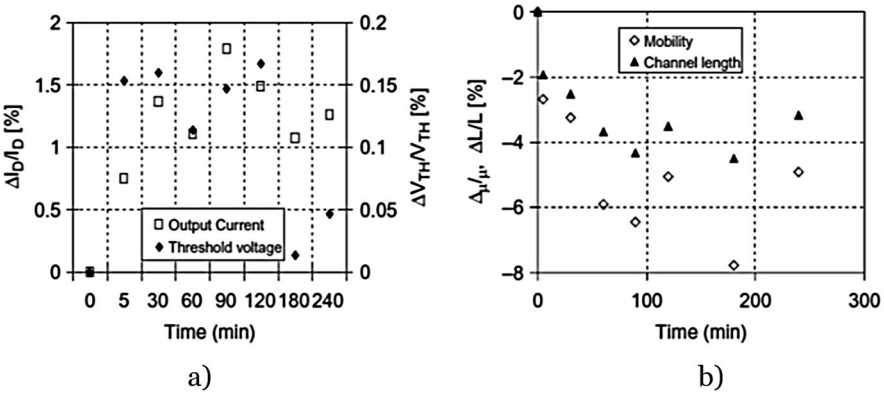

Fig. 5.2 Changes in CoolMOS transistor parameters during stress [1]. (**a**) displays changes in output current and threshold voltage over time in minutes. Output current is represented by squares and threshold voltage by diamonds. (**b**) illustrates changes in mobility and channel length over time in minutes

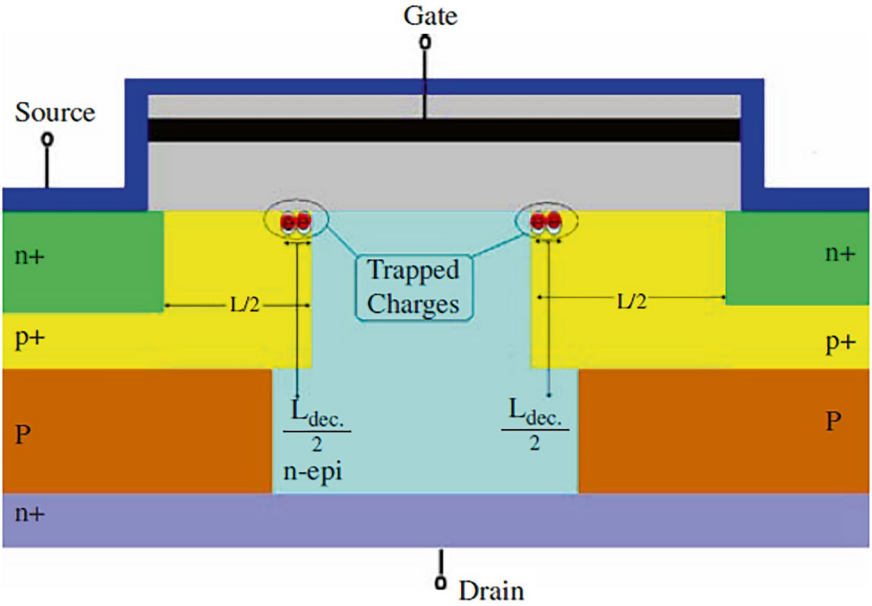

Fig. 5.3 Schematic representation of channel length decrease in CoolMOS transistor [1]

Mobility Decreasing Coefficient Extraction

We proposed a new mobility decreasing coefficient depending on the change in channel length, because of interface traps and trapped charges result in decrease both in mobility and channel length. We symbolized the mobility decreasing coefficient as C_r. The channel length decreasing region can be thought as rough region and the rest of the channel can be thought as smooth region. We defined the coefficient as the ratio of rough region to smooth region, and it is presented in Eq. (5.1):

$$C_r = \frac{A_{rg}}{A_t - A_{rg}} \tag{5.1}$$

where A_t is the channel size of the transistor and can be presented in Eq. (5.2):

$$A_t = W \cdot L \tag{5.2}$$

where W and L are the channel width and channel length, respectively. A_{rg} shows the rough region size, and it can be presented in Eq. (5.3):

$$A_{rg} = W \cdot L_{dec} \tag{5.3}$$

Here, L_{dec} is the channel length decrease. Hence, smooth region size can be found as A_t–A_{rg}. We put Eqs. 5.2 and 5.3 into Eq. (5.1) and rearranged the C_r as given in Eq. (5.4):

$$C_r = \frac{L_{dec}}{L - L_{dec}} \tag{5.4}$$

Change in C_r depends on stress is shown in Fig. 5.4.

The relation shown in Fig. 5.4 can be formulated as in Eq. (5.5):

$$C_r = 0.015\ln(t) + 0.008 \tag{5.5}$$

Decreasing mobility and C_r relation is shown in Fig. 5.5. Mobility decreases with the C_r as expected.

The relation shown in Fig. 5.5 can be formulated as in Eq. (5.6):

$$\frac{\Delta\mu}{\mu}[\%] = 100^{*}\left(\frac{\mu - \mu(0)}{\mu(0)}\right) = -76.76C_r + 0.24 \tag{5.6}$$

It is seen in Eq. (5.6) the mobility decreases linearly with C_r. For time dependency of mobility decrease, we put Eq. (5.5) into Eq. (5.6) and extracted Eq. (5.7):

$$\frac{\Delta\mu}{\mu}[\%] = -\left[1.15\ln(t) + 0.37\right] \tag{5.7}$$

We calculated the mobility change using Eq. (5.7) and compared it with the experimental results. As shown in Fig. 5.6, calculated and experimental results are in a good agreement.

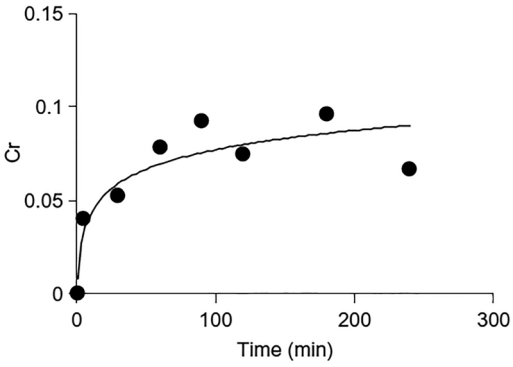

Fig. 5.4 Change in C_r with stress time [1]

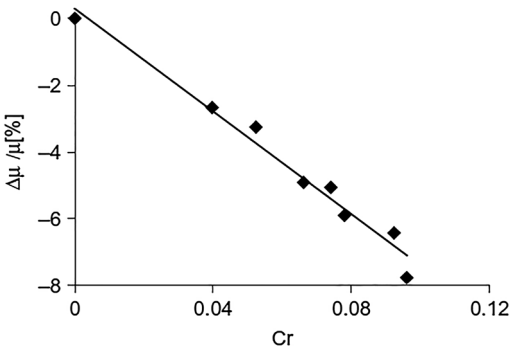

Fig. 5.5 Mobility decrease and C_r relation [1]

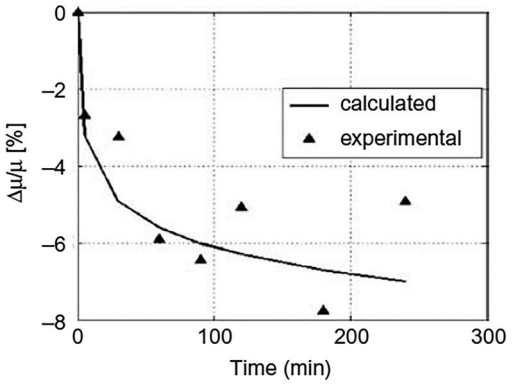

Fig. 5.6 Calculated and experimental results of mobility decreasing [1]

Concluding Remarks

We described an electrical stress-induced mobility degradation model for MOS transistors. For this purpose, we degraded power MOSFETs with electrical stress and determined the stress-induced changes in transistor parameters. We introduced a quantity C_r (mobility decreasing coefficient) which provides accurate models and predicts the mobility degradation in time independently from effects of process or operational changes such as oxide thickness, substrate doping, and applied voltages on transistor. We calculated the mobility change using proposed model and compared it with the experimental results. We saw that calculated and experimental results are in good agreement.

Investigation of Degraded Power MOSFET Effects on the Performance of DC–DC Converters Using Statistical Methods

Basic Concept

The use of a statistical approach for reliable and optimal design of systems, including electronic systems, has become quite popular. Statistically designed experiments/simulations have been used extensively for estimating or demonstrating existing reliability by identifying the important parameters (factors) affecting reliability out of many potentially important ones [11, 12]. This statistical approach ensures the performance and safety of critical electronic systems employed for space, nuclear, automotive, weapons, submarine and aerospace applications, to name a few [13]. In this study, degraded transistor effects on buck (step-down) and boost (step-up) converters including power MOSFET switch are analyzed. The analysis is based on a statistical approach of change in the output voltage of the converters owing to stress-induced change in the characteristic parameters of the power MOSFET. To perform this, power MOSFETs were degraded by applying high-voltage stress, experimentally. Stress-induced changes in threshold voltage, mobility, and channel length were determined. The simulations performed to investigate converter circuit performance are designed using the Taguchi method. The Taguchi method realizes a schedule of the simulations to obtain the most accurate information for a specific problem with a minimum number of experiments to qualify electronic systems against variations in the input parameters, environmental stresses and changing operating conditions [11]. The significance levels of transistor parameters change effects on converters are determined by investigating simulation results with ANOVA. The statistical analysis of variance (ANOVA), used in the Taguchi method, is adopted mainly to evaluate the significance level of every factor response and interpret observed data [14].

Materials and Method

Buck and Boost Converters

The switch-mode DC–DC converters have become a common building block in modern battery-operated portable systems. The voltage supplied by the battery and alternator is not adequate and first needs to be converted to the correct voltage level. DC–DC converters have many industrial applications, e.g., telecom power supplies, high-voltage generators, automotive, aircraft, inductive heating [2, 15–20]. Figure 5.7 shows the schematic for a basic step-down, or buck, DC–DC power converter.

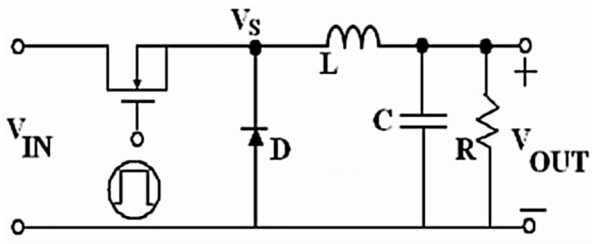

Fig. 5.7 Open-loop buck converter circuit diagram [2]

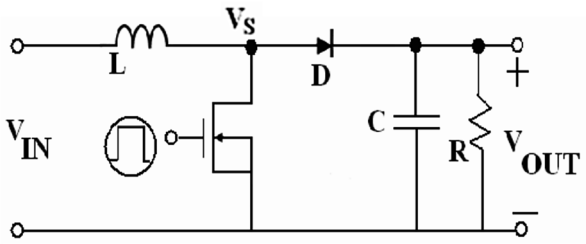

Fig. 5.8 Open-loop boost converter circuit diagram [2]

The converter considered here was designed to switch at a frequency of 250 kHz. In Fig. 5.7, V_{IN} = 5 V, V_{GATE} = 5 V, L = 9.9 µH, C = 20 µF and R = 1 kΩ. Figure 5.8 shows the circuit diagram for the second power converter, which is used to step-up an input voltage, hence the name boost converter. Boost converter is designed by using same components in buck converter.

In the converter circuits, n channel vertical power MOSFET transistor STP9NK70ZFP, in TO-220FP package in insulated version, built in standard Si-gate technology and produced by ST Microelectronics, was used. Its current and voltage ratings are 7.5 A and 700 V, respectively. The basic quantities of the transistors are given as W = 1 µm, L = 1 µm, t_{ox} = 1050 Å, μ = 500 cm²/V s, V_{TH} = 4.782 V by the manufacturer.

Taguchi Method

The statistical experiments/simulations can be planned in four ways: (1) trial and error; (2) one factor at a time experiments; (3) full-factorial experiments; and (4) Taguchi's orthogonal arrays (OA) [18].

Orthogonal arrays can eliminate the bias produced by one factor at a time experiments and improve the experimental efficiency of full-factorial experiments. Based on the principle of maintaining the accuracy of experiment results, the use of orthogonal arrays can considerably reduce the time required to perform the experiments and increases the reproducibility of the experiment results [14]. Therefore, orthogonal arrays are applied herein to perform simulation plan. We used L9 orthogonal array three factors at three levels and orthogonal array is set as given in

Table 5.1. Taguchi method considers the output response of a system due to the variations of control factors [11]. The methodology of Taguchi applied in this study is represented in Fig. 5.9.

ANOVA

Analysis of variance (ANOVA) is a powerful statistical technique to evaluate the significance level of every factor response. After the ANOVA test is performed, the analyst is able to perform further analysis on the systematic factors that are statistically contributing to the data set's variability. The equations used in the ANOVA statistical analysis in this study are as follows [9]. The equations are given for factor A and can be applied to the other factors. Sum of squares of factor A is calculated using Eq. (5.8).

$$\mathrm{SS}_A = \left(\sum_{i=1}^{k_A} \frac{A_i^2}{n_{A_i}} \right) - \frac{T^2}{N} \tag{5.8}$$

Here, SS_A is the sum of squares of the factor A, k_A is the number of the levels of factor A, A_i is the sum total of the experimental results at level i of factor A, n_{Ai} is the number of all experimental results at level i of factor A, T is the sum of all experimental results, and N is the number of all experiments. Total sum of squares is calculated using Eq. (5.9).

$$\mathrm{SS}_T = \sum_{j=1}^{N} y_j^2 - \frac{T^2}{N} \tag{5.9}$$

Here, SS_T is the total sum of squares and y_j is the experimental result of jth trial. The sum of squares of error is calculated using Eq. (5.10)

$$\mathrm{SS}_e = \mathrm{SS}_T - \left(\mathrm{SS}_A + \mathrm{SS}_B + \cdots \right) \tag{5.10}$$

Table 5.1 L9 orthogonal array [2]

Experiment	A	B	C
1	Level 1	Level 1	Level 1
2	Level 1	Level 2	Level 2
3	Level 1	Level 3	Level 3
4	Level 2	Level 1	Level 2
5	Level 2	Level 2	Level 3
6	Level 2	Level 3	Level 1
7	Level 3	Level 1	Level 3
8	Level 3	Level 2	Level 1
9	Level 3	Level 3	Level 2

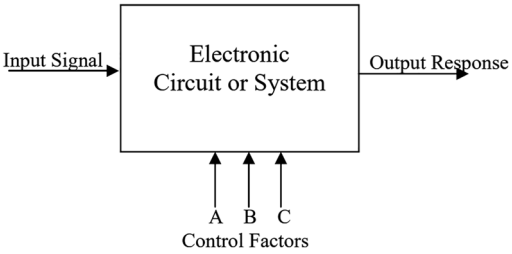

Fig. 5.9 The methodology of Taguchi applied in this study [2]

Here, SS_e is the sum of squares of error. Degree of freedom (DOF) is defined as number of independent comparisons to make inferences. DOF of a factor equals to minus 1 of level number of the factor in orthogonal array. The total DOF equals minus 1 of the number of trials in orthogonal array. Mean sum of squares (Variance) of each factor is calculated using Eq. (5.11).

$$\mathrm{MSS}_A = \frac{\mathrm{SS}_A}{\mathrm{sd}_A} \tag{5.11}$$

Here, MSS_A is the variance of factor A and DOFA is the degrees of freedom of factor A. We exploit the F-ratio of the factor to decide whether the factor is significance or not on the output response of the system. The F-ratio is calculated using Eq. (5.12).

$$F_A = \frac{\mathrm{MSS}_A}{\mathrm{MSS}_e} \tag{5.12}$$

Here, F_A is the F ratio of factor A and MSS_e is the variance of error. Percent contribution ($\%p$) represents the relative impact of factors on the output response. Percent contribution of factor A is calculated using Eq. (5.13).

$$p_A(\%) = \frac{\mathrm{SS}_A}{\mathrm{SS}_T} \tag{5.13}$$

Experimental Results

Firstly, the power MOSFET under test is stressed by electrical stress with the gate bias of $V_G = 40$ V (source and drain were grounded) at ambient temperature for 4 h, representing high-voltage stress. We investigated the changes in transistor parameters and determined high-voltage stress-induced changes in threshold voltage (V_{TH}), mobility (μ), and channel length (L) during the stress [20]. The threshold voltage is changed between [0.13–0.9%], mobility changed between [2.43–26.3%], and channel length changed between [2–20.2%] intervals during the stress. We selected the V_{TH}, μ, and L as control factors and applied the Taguchi method to design simulations. The control factors and factor levels values are given in Table 5.2.

We determined the factor levels from the experimental results as the smallest (Level 1), average (Level 2), and the largest (Level 3). We simulated the converters using this factor levels in Table 5.1.

Simulation Results

At first, we simulated the buck and boost converters at different operating conditions to extract the behavior of degraded transistor effects on converters at different operating conditions. We changed the model parameters of the transistor given by manufacturer in PSPICE using experimental results to simulate the stress effect. The stress-induced change in converters output voltage for different V_{IN} and V_{GATE} values are given in Table 5.3.

As given in Table 5.3, the degraded transistors have a significant effect on the converter output voltages especially for $V_{GATE} = 5$ V. When the gate voltage increased to 6 V, buck converters output voltage changes but there is no change at boost converters. After that, we performed the simulations on the buck converter at operating condition #1 according to Taguchi design. We calculated relative changes in the output voltage. The simulation results are given in Table 5.4.

We used simulation results for ANOVA to identify the most effective transistor parameter change effecting converter output. The ANOVA results are given in Table 5.5.

High-voltage-induced change in the threshold voltage of the power MOSFET has dominant effect on the change in buck converter output voltage as given in Table 5.5. Changes in the mobility and channel length have negligible effects on the change in buck converter output voltage. To realize the degraded transistor parameters effects at different operating conditions on converter output voltage, we

Table 5.2 Control factors and level values [2]

Control factors	Description	Level 1	Level 2	Level 3
A	Threshold voltage (V_{TH}) (V)	4.788	4.8	4.825
B	Mobility (μ) (cm^2/V s)	512.1	570.75	631.5
C	Channel length (μm)	1.02	1.11	1.2

Table 5.3 Change in output voltage of converters at different operating conditions [2]

Operating conditions			$\frac{\Delta V_{OUT}}{V_{OUT}}[\%]$	
	V_{IN}	V_{GATE}	Buck	Boost
#1	5	5	−20	−20
#2	6	6	−3.6	0
#3	6	5	−20	−17.7
#4	5	6	−3.6	0

Table 5.4 Change in the output voltage of the buck converter at operating condition #1 [2]

Experiment number	$\frac{\Delta V_{OUT}}{V_{OUT}}[\%]$
#1	−2.25
#2	−2.17
#3	−2.11
#4	−7.82
#5	−7.71
#6	−6.9
#7	−20.36
#8	−19.72
#9	−19.69

Table 5.5 ANOVA results for output voltage of buck converter for operating condition #1 [2]

Factors	DOF	SS	MSS	*F*-ratio	*%p*
V_{TH}	2	497.95	248.97	46,297.35	99.83
μ	2	0.49	0.24	46.40	0.10
L	2	0.29	0.14	27.08	0.05
Error	2	0.01	0.0053		
Total	8	498.75			

Table 5.6 Change in the output voltage of the buck converter at operating condition #2 [2]

Experiment number	$\frac{\Delta V_{OUT}}{V_{OUT}}[\%]$
#1	−0.52
#2	−0.45
#3	−0.36
#4	−1.53
#5	−1.53
#6	−1.26
#7	−3.78
#8	−3.51
#9	−3.42

simulated the buck converter at operating condition #2 according to Taguchi method. We calculated relative changes in the output voltage. The simulation results are given in Table 5.6.

We used simulation results for ANOVA to identify the most effective transistor parameter change effecting converter output at operating condition #2. The ANOVA results are given in Table 5.7.

For operating condition #2, also, high-voltage-induced change in the threshold voltage of the power MOSFET has dominant effect on the change in buck converter output voltage as given in Table 5.7. Consequently, the change in the threshold

Table 5.7 The ANOVA results [2]

Factors	DOF	SS	MSS	*F*-ratio	*%p*
V_{TH}	2	15.30	7.65	10,280.34	99.14
μ	2	0.10	0.052	70.313	0.67
L	2	0.02	0.012	17.11	0.16
Error	2	0.0014	0.0007		
Total	8	15.43			

Table 5.8 Change in the output voltage of the boost converter at operating condition #1 [2]

Experiment number	$\frac{\Delta V_{OUT}}{V_{OUT}}[\%]$
#1	−3.01
#2	−1.54
#3	−0.08
#4	−13.84
#5	−7.68
#6	−3.1
#7	−27.72
#8	−17.14
#9	−16.37

Table 5.9 ANOVA results for output voltage of boost converter for operating condition #1 [2]

Factors	DOF	SS	MSS	*F*-ratio	*%p*
V_{TH}	2	580.67	290.33	120.67	71.46
μ	2	164.002	82.001	36.05	20.18
L	2	63.26	31.63	13.91	7.78
Error	2	4.54	2.27		
Total	8	812.49			

voltage of the power MOSFET has dominant effect on the change in buck converter output voltage and the operating conditions do not change the degraded transistor effects on buck converter output voltage. We also simulated the boost converters at operating condition #1 according to Taguchi design. The calculated relative changes in the output voltage are given in Table 5.8.

We used simulation results in Table 5.8 for ANOVA and results are given in Table 5.9. For boost converter, change in the threshold voltage of the power MOSFET is the major effect on the change in boost converter output voltage as given in Table 5.9. The effects of the changes in the mobility and channel length cannot be neglected in boost converter output voltage differently the buck converter. As a result, degraded device placement in a circuit is very important for reliability of the circuit. The statistical investigation of boost converter at operating condition #2 has not been performed, because there is no change in the output voltage.

Concluding Remarks

In this section, degraded power MOSFET effects on buck and boost converters including power MOSFET switch are investigated using statistical methods. The changes in the experimentally degraded power MOSFET parameters were used as control factors and converter circuits simulated according to Taguchi design. The ANOVA is used to evaluate the significance level of degraded power MOSFET parameters. The change in the threshold voltage dominates the change in the converter circuit output voltage. Degraded device placement in a circuit is very important for reliability of the circuit. The operating conditions can suppress the degraded device effects, so it is very important for reliability.

High-Voltage Stress Effects on Power MOSFETs in Switching DC–DC Converters

Basic Concept

The switch-mode DC–DC converters have become a common building block in modern battery-operated portable systems. Small form factor, high robust stability, fast transient response, high efficiency, and low cost are the most desired performances for DC–DC converters [3]. Switched-mode power converters operate in a manner that is much more efficient than their linear converter counterparts. In a switched-mode power converter, the controlling device is a switch, which continually opens and closes [21]. DC–DC converters have many industrial applications, e.g., telecom power supplies, high-voltage generators, automotive, aircraft, inductive heating [17, 20, 22–34]. On the other hand, there is increasing worldwide interest in sustainable energy production and use, there is renewed focus on the power electronic converter interface for DC energy sources. Three specific examples of such DC energy sources that will have a role in distributed generation and sustainable energy systems are the photovoltaic (PV) panel, the fuel cell stack, and batteries of various chemistries [25–28]. Each system can be discussed from technical, economical, and reliability viewpoints. In large factories, the lifetime and the number of failures and associated cost for a system are estimated using the reliability of the system. If a system is acceptable from technical point of view but has low reliability, it would not be practical to use it, and the investment will not be done on such a system. It also affects the electrical safety of the systems. Due to environmental concerns, more effort is now being put into the clean distributed power like geothermal, solar thermal, photovoltaic, and wind generation as well as fuel cells. The reliability of DC–DC converters has been calculated and the optimum topology has been presented from reliability point of view [29–33].

In this study, high-voltage degradation of buck (step-down) and boost (step-up) converters which include power MOSFET switch were investigated. To perform

this, power MOSFETs were degraded by applying high-voltage stress from the gate terminal and stress-induced output current, threshold voltage, mobility and channel length changes were determined. Converter circuits were simulated before and after power MOSFET degradation for two different input voltages. Degraded transistor effects on converter circuits were determined by investigating circuit performance.

Experiment Platform and Procedure

Same circuits and component values are used for investigation shown in Figs. 5.7 and 5.8.

Results and Discussion

The power MOSFET under test is stressed by electrical stress with the gate bias of $V_G = 40$ V (source and drain were grounded) at ambient temperature, representing high-voltage stress. It is aimed to apply stress that will not break the gate oxide but it will generate traps is gate oxide and interface. When power MOSFET operates in saturation, drain current can be expressed by Eq. (5.14):

$$I_D = \frac{\beta}{2}\left(V_{GS} - V_T\right)^2 \tag{5.14}$$

where β is the gain factor ($\beta = \mu\ C_{OX}$ W/L) and V_{TH} is the threshold voltage. In expression for gain factor, μ is the channel carrier mobility, C_{OX} is the gate oxide capacitance per unit area, while W and L are the channel with and length, respectively. During the stress, I_D–V_{DS} and I_D–V_{GS} measurements recorded in time interval. Corresponding values of threshold voltage were determined by extrapolation of linear parts of transfer characteristics to intersections with V_G axis ($I_D = 0$), while corresponding values of mobility were determined from slopes of linear parts of measured transfer characteristics of power MOSFET during stress [34]. The output current change was determined by using I_D–V_{DS} curve. Channel length change is determined by using Eq. (5.14). All of the parameter changes put into Eq. (5.14) and channel length change was extracted [20]. The parameter changes of power MOSFET depending on stress time are shown in Figs. 5.10, 5.11, 5.12, 5.13, 5.14, and 5.15.

The voltage and current changes of the converter circuits components were also examined. In Fig. 5.16, $I_D(M)$ drain current of power MOSFET, V_S node voltage shown in Figs. 5.7 and 5.8, t_r rise time of the converter circuits, I_{OUT} output current of the converters, I_L output current of the inductor, I_C output current of the capacitance, V_L voltage across the inductor, P_{OUT} output power of the converters, P_M power dissipation of the power MOSFET.

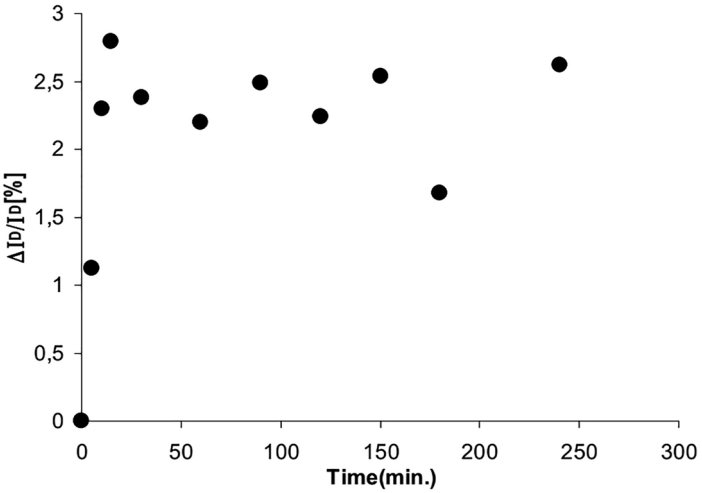

Fig. 5.10 Dependence of power MOSFET's output current on stress time [3]

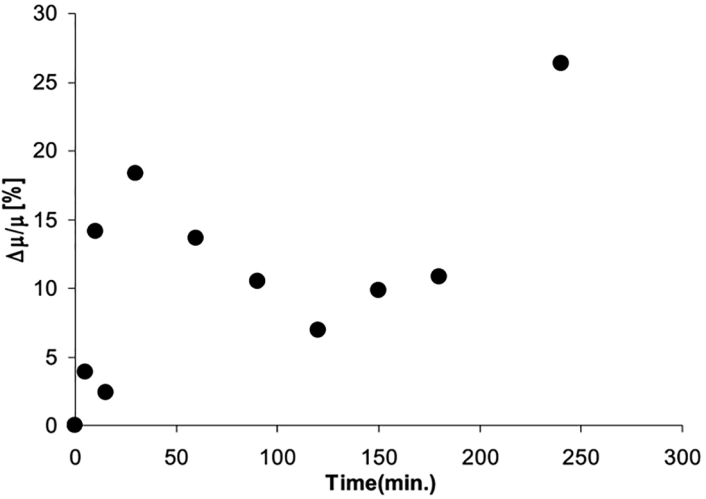

Fig. 5.11 Dependence of power MOSFET's mobility on stress time [3]

In Figs. 5.16 and 5.17, parameter changes are shown for buck and boost converters at V_{IN} = 5 V, respectively. It is seen that parameters of the converter circuits reduce with the degraded power MOSFET switch, except rise time. The rise time of the circuits is increased. The interesting point is the output current of the power MOSFET is increased after the stress, but it reduced in the converter circuits. The

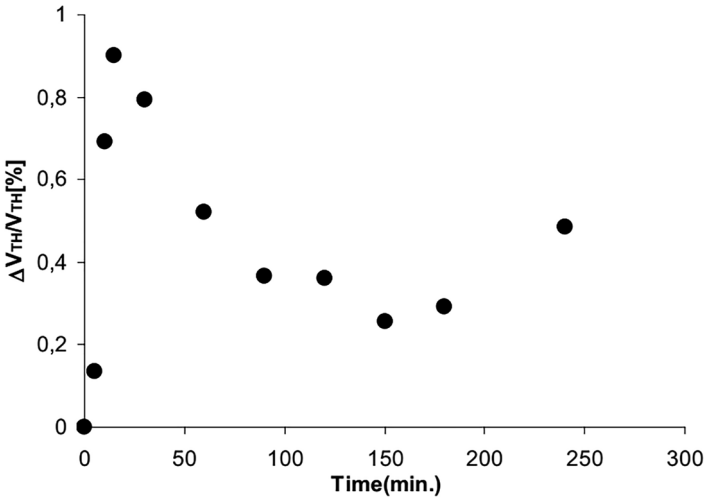

Fig. 5.12 Dependence of power MOSFET's threshold voltage on stress time [3]

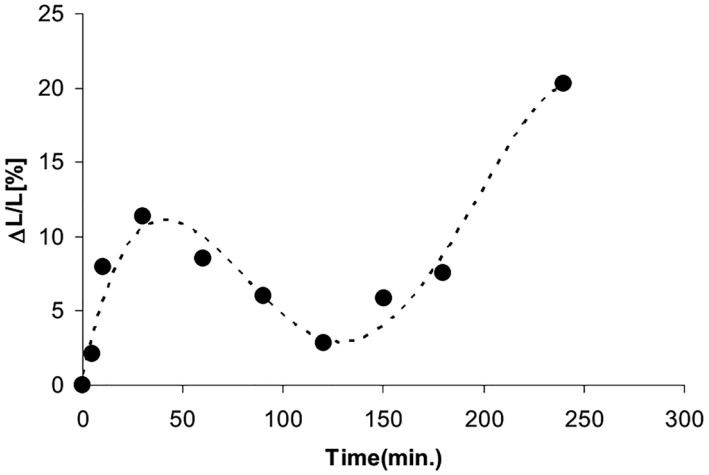

Fig. 5.13 Dependence of power MOSFET's channel length on stress time [3]

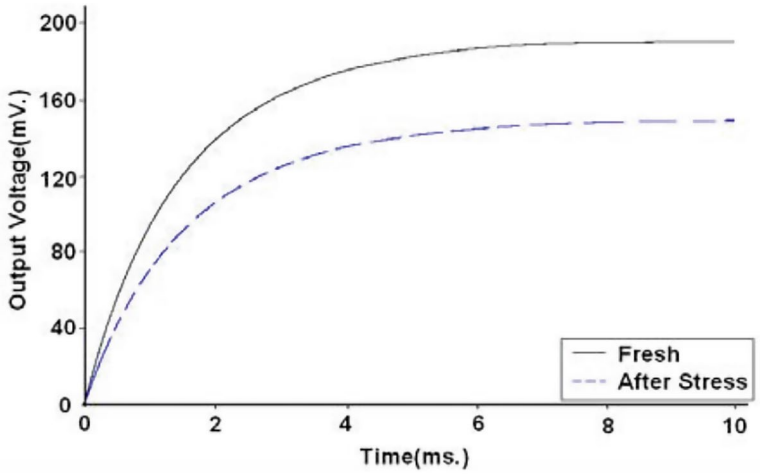

Fig. 5.14 Change in buck converter output voltage before and after the stress (V_{IN} = 5 V) [3]

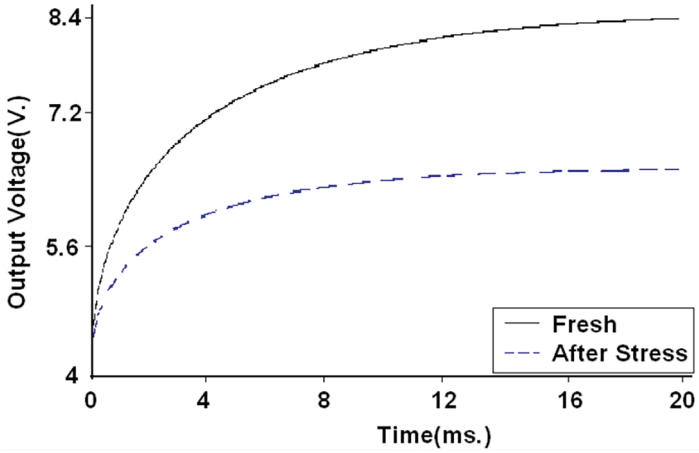

Fig. 5.15 Change in boost converter output voltage before and after the stress (V_{IN} = 5 V) [3]

converter circuits were also simulated at V_{IN} = 6 V. Parameter changes were observed in buck converters but in boost converters there were negligible parameter changes. The parameters changes of buck converter at V_{IN} = 6 V are seen in Fig. 5.18.

In Fig. 5.18, it is seen that the parameter changes are smaller according to Fig. 5.16. Power dissipation of the power MOSFET is increased at V_{IN} = 6 V and rise time of the buck converter reduced. It is also examined that which parameter changes of the power MOSFET has a major effect on converter parameter changes. For this purpose, parameter changes of the power MOSFET were applied to Spice

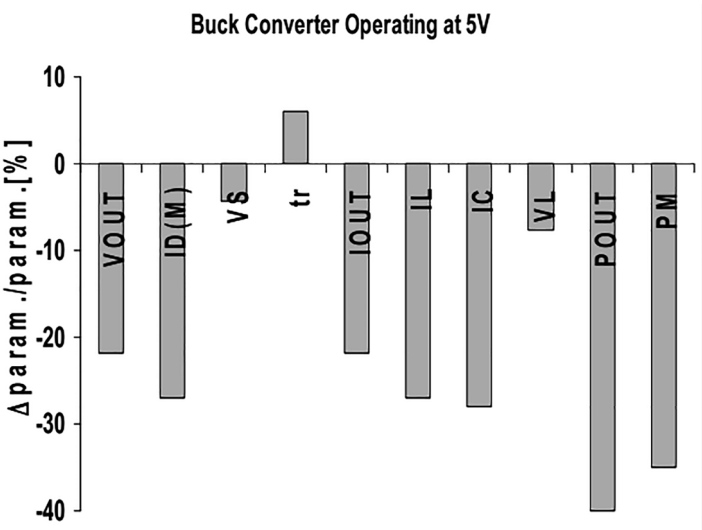

Fig. 5.16 Change in buck converter parameters before and after the stress (V_{IN} = 5 V) [3]

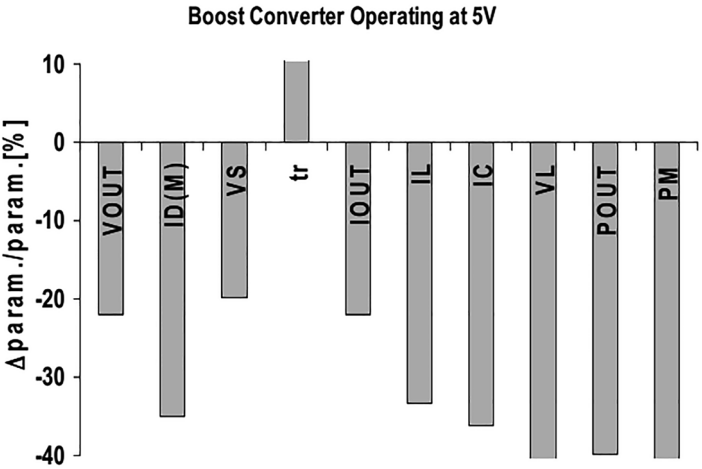

Fig. 5.17 Change in boost converter parameters before and after the stress (V_{IN} = 5 V) [3]

parameters one by one and circuit simulations were performed for each. It is note that the most effective power MOSFET parameter on converter circuit performance is the threshold voltage. It also explains why the converter parameter changes are smaller at V_{IN} = 6 V. When input voltage increases, the threshold voltage change gets smaller according to operating conditions and its effect on converter reduces.

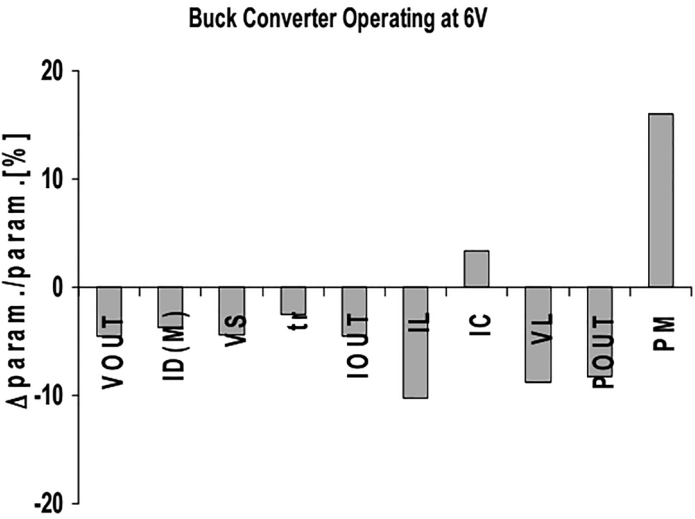

Fig. 5.18 Change in buck converter parameters before and after the stress (V_{IN} = 6 V) [3]

Concluding Remarks

In this section, high-voltage stress effects on power MOSFET switching buck and boost converters were examined. Firstly, power MOSFET was degraded experimentally and change in transistor parameters were determined. Changes in parameter were adapted to transistor's Spice parameters. Converter circuits' simulations were performed before and after the stress. Node voltages, component currents, and power dissipations in circuits were analyzed. It is seen that the output voltage of the converters reduced after stress. When the input voltage increased, the changes in circuit parameters were smaller. It was also determined that the most effective power MOSFET parameter on converter circuit performance is the threshold voltage.

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